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Contents

Comparing Netlists 6

The *Netlist Comparison* tool in the Design Manager module allows you to compare schematic and PCB databases and produce reports showing the differences in electrical connectivity between two netlists.

There are two ways to compare and report the differences in electrical connectivity between two netlists:

- You can run *Netlist Comparison* by selecting the button on the opening screen and choosing options on the Netlist Comparison screen.
- You can run a netlist from the DOS prompt by using the command line mode.

The advantage of running *Netlist Comparison* from within the Design Manager module is that the system automatically extracts netlist information from a schematic or PCB file and creates an expanded netlist for multisheet designs when necessary.

Command line mode lets you run the program by entering options on the command line, at the DOS prompt. These options are the netlists, the part filenames, and the reports to produce. After you enter the command line, the system runs automatically with no further input from you.

Running from the command line is useful if you want to process several different sets of netlists in one or more designs by using a batch process. No automatic netlist generation, extraction, or linking occurs when you use the command line mode to compare netlists.

You can compare netlists during the design process to check revision updates and show discrepancies in your PCB designs.

This chapter presents the following information:

- using the *Netlist Comparison* tool to

— `compare two schematics`
— `compare two PCB layouts`
— `compare a schematic to a PCB layout`
— `view and print netlist comparison reports`

- using the command line mode to compare netlists and print reports

Using the *Netlist Comparison* Tool

The *Netlist Comparison* tool automatically extracts and links netlists from schematic and PCB databases and produces an ASCII report file (.nlc) showing the differences in electrical connectivity between the two netlists.

The system assigns names to unnamed components (UC) and unnamed nets (UN); for example, UC00000001 and UN00000001. The system assigns these names to any component in the database that doesn't have a user–assigned name. This automatic naming takes place when the system automatically extracts the netlist for the PCB database or when unnamed components are entered into a schematic database. Assigning system–generated names guarantees uniqueness for all nets and components in the database.

You can assign your own component and net names by using any of the Name commands in the Schematic Editor or the PCB Editor.

When you compare netlists, you have the option of comparing user–assigned component and net names while the system compares net connectivity to component pins. When the component and name checking option is enabled, the system ignores the system–assigned names when you run a netlist comparison, but the names still appear in the report. When the component and name checking option is disabled, the system only checks and matches the gates and nets in the two netlists. Only the system–assigned component and net names are listed in the report.

The system default is to run *Netlist Comparison* without component and net name checking.

Opening the Netlist Comparison Screen

To open the Netlist Comparison screen from the P–CAD opening screen, select the *Design Manager* button. The button is highlighted and the *Design Manager* tool buttons are available for selection.

To open the Netlist Comparison screen

- Select *Netlist Comparison.* You'll see the Netlist Comparison screen shown in Figure 6-1.

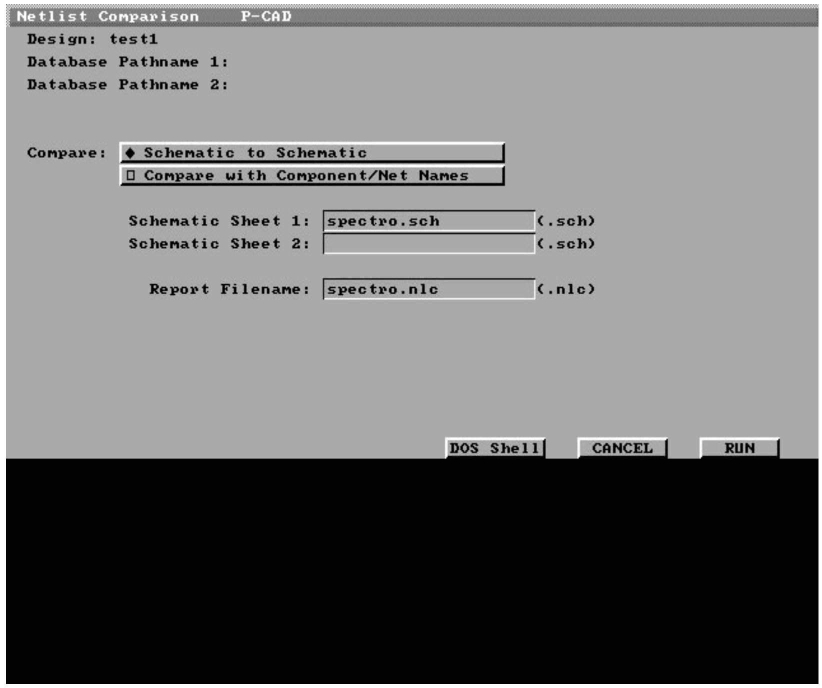

Figure 6-1. Netlist Comparison Screen

Comparing Two Schematics

When comparing two schematic netlists, *Netlist Comparison* compares and attempts to match the gates and nets in both netlists. When comparing single netlists extracted from a single schematic sheet, *Netlist Comparison* automatically creates a schematic netlist file (.nlt). When comparing multiple schematic sheet designs, *Netlist Comparison* extracts a netlist from each sheet in the design and then links them to form an expanded netlist (.xnl).

You can also use an annotated schematic netlist (.bnl) that you can (optionally) produce when you package the schematic. You can later use the *Engineering Change Order (ECO)* tool to back–annotate the schematic netlist.

During the comparison, the following gate characteristics are checked:

- number of pins
- pin numbers of net connections
- connecting nets

- component or net names (optional)
- packaging information

During the comparison, the following net characteristics are checked:

- number of pins
- pin numbers of net connections
- connecting gates
- net names (optional)

To compare two schematic netlists

1. Cycle to *Schematic to Schematic*.
2. Fill the Compare With Component/Net Names check box to produce a report that includes component and net names checking.
3. Select the Schematic Sheet 1 data entry box.
4. Enter the schematic sheet filename in the data entry box on the file selector screen if you want a name other than the default filename.

   or

   Select a schematic sheet filename from the file selector list box. (The default sheet filename for the Schematic Sheet 1 data entry box is always the currently selected sheet on the P–CAD opening screen.)
5. Select *OK*.
6. Select the Schematic Sheet 2 data entry box.
7. Enter the second schematic sheet filename in the data entry box on the file selector screen.

   or

   Select a schematic sheet filename from the file selector list box.
8. Select *OK*.
9. Select the Report Filename data entry box.

10. Enter the name of the output report filename if you want a name other than the default filename. (The default output report filename is the same as the Schematic Sheet 1 filename.)

11. Select *RUN.*

The Netlist Comparison screen closes. *Netlist Comparison* automatically processes and compares the two netlists and creates the output report (.nlc). Errors and status messages are sent to pcad.log. Refer to the *Error Messages* manual for an explanation of the status messages and any error messages.

Comparing Two PCB Layouts

Two PCB layout netlists can be compared to check for continuity changes made to either PCB netlist. *Netlist Comparison* automatically extracts a packaged netlist (.pnl) from the specified PCB layout.

Note: *Netlist Comparison* checks net connectivity established by the ratsnest connections. To verify and report connectivity made by the actual wire connections in the PCB, you can run the DRC tool. For details, see the section on checking for design rules violations in the *PCB Tools* manual.

When it's comparing two PCB netlists, *Netlist Comparison* compares and attempts to match the parts and nets in both netlists. The following part characteristics are checked:

- number of pins
- pin numbers of net connections
- connecting nets
- part names (optional)
- packaging information

The following net characteristics are checked:

- number of pins
- pin numbers of net connections
- connecting parts
- net names (optional)

To compare two PCB layouts

1. Cycle to *PCB to PCB*.
2. Fill the Compare With Component/Net Names check box to produce a report that includes component and net names checking.
3. Select the PCB Layout 1 data entry box if you want to enter a PCB layout other than the default.
4. Enter a PCB layout filename in the data entry box on the file selector screen.

   or

   Select a PCB layout filename in the file selector list box. (The default PCB filename is the same as the currently active PCB layout on the P–CAD opening screen.)
5. Select *OK*.
6. Select the PCB Layout 2 data entry box.
7. Enter a PCB layout filename in the data entry box on the file selector screen.

   or

   Select a PCB layout filename from the file selector list box.
8. Select *OK*.
9. Select the Report Filename data entry box.
10. Enter the name of the output report filename if you want to enter a name other than the default filename. (The default output report filename is always the same as the PCB Layout 1 filename.)
11. Select *RUN.*

The Netlist Comparison screen closes. *Netlist Comparison* automatically processes the two netlists and creates the output report (.nlc). Status messages and any error messages are sent to pcad.log. Refer to the *Error Messages* manual for an explanation of the error messages.

Comparing a Schematic to a PCB Layout

When comparing a schematic netlist to a PCB netlist, *Netlist Comparison* compares the gates and the nets in both netlists. The following gate characteristics are checked:

- number of pins
- pin numbers of net connections
- connecting nets
- reference designators
- packaging information
- pin LEQs (logical equivalence codes)

The following net characteristics are checked:

- number of pins
- pin numbers of net connections
- connecting gates

Two input files are required when you want to compare a schematic to a PCB:

- a schematic netlist (required)
- a PCB netlist (required)
- a cross–reference file (optional)

The input schematic netlist can be one of the following:

- a single–sheet netlist (.nlt)
- a multisheet netlist that has been linked together (.xnl)
- an annotated schematic netlist that results from packaging a schematic and updating the netlist using the *Engineering Change Order (ECO)* tool. An input PCB netlist is a packaged netlist extracted from the PCB database (.pnl).

When comparing a schematic netlist to a PCB netlist, the Compare With Component/Net Names option isn’t available. The system doesn’t check for mismatched user–assigned gate and part names in this type of comparison.

Packaging Information and Reference Designators

A schematic–to–PCB netlist comparison checks for packaging inconsistencies as well as differences in connectivity between the two netlists. Because packaging is checked, the system must know which physical PCB part each gate in the schematic is assigned to. Reference designators are used to identify which gate symbols belong to which corresponding part packages, but the system must be able to find a part file for each symbol file.

There are three ways to specify which symbol file will be packaged into a part file:

- The easiest way to specify which symbol files are packaged into a part file is to give the symbol and part file the same base filename. For example, 7400.sym could be packaged into a 7400.prt file.
- You can also assign the attribute PRT= to the symbols in the schematic to specify which part file is used. This way, you can package a 74ls04.sym into a 7404.prt outline.
- When using nonhomogeneous parts (or in other situations where using the same filename or an attribute isn't practical), you can create a cross–reference file (.fil) that maps symbols to parts in an ASCII format. This file is specified on the Design Maintenance screen. (See Chapter 2, "Maintaining Design Files" for more information about selecting cross–reference files. Also see the section on packaging schematics in the *Schematic Tools* manual for more information about cross–reference files.)

Before you can compare a schematic netlist to a PCB netlist, you need to make sure that the packaging information is the same for corresponding gates and parts and that reference designators have been assigned to all gates in the schematic.

To assign reference designators, you can do one of the following:

- Use *Enter*! *Ref. Des. & Section* in the Schematic Editor to assign the reference designators manually.
- Use *Engineering Change Order (ECO)* to back–annotate the schematic with reference designators that you resequenced while editing the PCB layout.

- Use *Package Schematic* to let the system automatically assign the reference designator for the PCB layout.
- Use *ECO* to back–annotate the schematic with system–assigned reference designators.

If packaging information is missing from a gate or part, *Netlist Comparison* processes the component as a single gate and lists the components in the netlist comparison output report.

To keep parts (such as mechanical parts) out of the comparison, *Netlist Comparison* looks for the attribute

COMPARE = MECH

If this attribute is assigned to a part file, it's listed separately in the output report. Parts you specify as jumpers by using *Enter* ! *Jumper* in the Part Editor are also listed separately.

Pin Logical Equivalency (LEQ) Values

In schematic–to–PCB netlist comparison, nets are compared by using pin LEQ values. If there are any inconsistencies between corresponding schematic and PCB pin LEQ values, the gate and part types with inconsistent pin LEQs are listed in the Gate Report portion of the output file.

When it compares pin LEQ values, *Netlist Comparison* assumes that the LEQ values for the component ID type of the symbol are correct. If an inconsistency is found, both the symbol and part component ID types are treated as having erroneous pin LEQ information.

For more information on component ID types and pin LEQ values, see the section on using the Symbol Editor in the *Library Manager* manual.

To compare a schematic to a PCB layout

1. Cycle to *Schematic to PCB*.
2. Select the PCB Layout data entry box to change from the default filename. (The default is the PCB layout currently selected on the P–CAD opening screen.)
3. Enter the PCB Layout filename in the data entry box on the file selector screen.

   or

   Select the PCB Layout filename in the file selector list box.

4. Select *OK*.

5. Select the Report Filename data entry box if you want to change the default. (The default report filename is the name of the current design directory.)

6. Enter the name of the netlist report filename.

7. Select *RUN.*

The Netlist Comparison screen closes. *Netlist Comparison* automatically processes the two netlists and creates the report (.nlc). Status messages and any error messages are sent to pcad.log. Refer to the *Error Messages* manual for an explanation of the error messages.

The following paragraphs show some examples of the types of reports you can produce when you compare netlists.

Viewing and Printing the Report

You can view and print the netlist comparison report (*filename*.nlc) by using the *Report Editor* tool described in Chapter 6.

Report Comparing Two Schematic Netlists

The Netlist Comparison report in Figure 6-2 was produced by comparing two schematic netlists. The report first summarizes the comparison results, and then lists components with missing packaging information, suspect gates, suspect nets, spare gates, and floating nets, as described below.

```
%*********************************************************************
%                                                                    *
%  Program        :  PC*NLC VERSION 8.5   Netlist Comparison *
%  Date           :  Aug 15 1995                                     *
%  Time           :  09:51:29                                        *
%  Netlist1       :  a.nlt                                           *
%  Netlist2       :  b.nlt                                           *
%  Comparison Made  :  WITH Gate Names                               *
%                                                                    *
%*********************************************************************

                nlc Report
                ----------

Netlist1: a.nlt                        Netlist2: b.nlt
Number of Gates              47        Number of Gates              47
Number of Nets              112        Number of Nets              112
Number of Suspect Gates       3        Number of Suspect Gates       3
Number of Suspect Nets        2        Number of Suspect Nets        2
Number of Spare Gates         2        Number of Spare Gates         2
Number of Floating Nets       3        Number of Floating Nets       3
```

Figure 6-2. Report Comparing Two Schematic Netlists

- *Number of Gates* reports the total number of gates in each netlist.
- *Number of Nets* reports the total number of nets in each netlist.
- *Number of Suspect Gates* reports the total number of gates that don’t match gates in the other netlist.
- *Number of Suspect Nets* reports the total number of nets that don’t match nets in the other netlist.
- *Number of Spare Gates* reports the total number of gates that aren’t connected to nets in each netlist.
- *Number of Floating Nets* reports the total number of nets that aren’t connected to gates in each netlist.

List of Components With Missing Packaging Information

Figure 6-3 shows the section of the report that lists components with missing packaging information; for example, 74ls32.sym and 74hs00.sym.

List of Suspect Gates

In the *List of Suspect Gates* section of the report, *Suspect Gates from Netlist1* (shown in Figure 6-3) reports the name of the first netlist (for example, a.nlt) and lists the gates in netlist 1 that don’t match other gates in netlist 2. Other details of this section of the report are described below.

- *From sheet/macro* reports the name of the schematic sheet or third–party macro that the gates are in (for example, ezboard).
- *Gate Type:Name* lists the gate types (base symbol filenames) and either the system–assigned name (for example, UC00000001) or the user–defined component names assigned by using *Name* ! *Component* in the Schematic Editor (for example, nand2).
- *Logical Pin Name* lists the logical pin names you assign to the symbols by using *Enter* ! *Pin* in the Symbol Editor (for example, INA).
- *Net Name* lists the names of the nets connected to the pins. Net names are automatically assigned when you use *Name* ! *Wire* (for example, UN00000001), or you can assign your own by using *Name* ! *Net* in the Schematic Editor (for example, +5V).
- *Physical Pin Num* lists the physical pin numbers you assign to the gate by using *Enter* ! *Ref. Des. & Section* in the Schematic Editor (for example, 1).
- *Reference Designator* lists the names you assign to the gates by using *Enter* ! *Ref. Des. & Section* in the Schematic Editor (for example, U1).
- *Total Number of Suspect Gates from sheet/macro* reports the total number of gates (in this sheet or macro) that don’t match other gates in netlist 2 (for example, 3).

Suspect Gates from Netlist2 reports the name of the second netlist; for example, b.nlt, and lists the gates in netlist 2 that didn’t match other gates in netlist 1. The field descriptions are similar to those in *Suspect Gates from Netlist1* described previously in this section.

```
==============================================================
 List of Components with Missing Packaging Information:
==============================================================
    74ls32.sym    74hs00.sym


==============================================================
          List of Suspect Gates
==============================================================

 Suspect Gates from Netlist1:  a.nlt

  From sheet/macro:  ezboard

  Gate          Logical   Net      Physical   Reference
  Type:Name       Pin Name  Name      Pin Num    Designator
  -----       ----  ---    ----- -----

  nand2:A1       INA     = UN00000001   1     U1
             INB     = UN00000002   2
             OUTY    = QA1        3

  nand2:A2       INA     = UN00000003   4     U1
             INB     = UN00000004   5
             OUTY    = QA2        6

  nand2:A3       INA     = UN00000005   10    U1
             INB     = UN00000006   9
             OUTY    = QA3        8

   Total Number of Suspect Gates from sheet/macro:   3

 Suspect Gates from Netlist2:  b.nlt

  From sheet/macro:  ezboard

    Gate               Logical     Net      Physical     Reference
    Type:Name          Pin Name    Name     Pin Num      Designator
  -----              -----       ---      ----         -----


  nand2:B1       INA     = UN00000001   1     U1
             INB     = UN00000002   2
             OUTY    = QA1        3

  nand2:B2       INA     = UN00000003   4     U1
             INB     = UN00000004   5
             OUTY    = QA2        6

  nand2:B3       INA     = UN00000005   10    U1
             INB     = UN00000006   9
             OUTY    = QA3        8

   Total Number of Suspect Gates from sheet/macro:   3
```

Figure 6-3. Missing Packaging Information and Suspect Gates

List of Suspect Nets

The *List of Suspect Nets* section of the report, shown in Figure 6-4, describes differences when the same nets in the two netlists aren't identical. For example, in netlist 1, net A is connected to U10 pin 1.

In netlist 2, net A is connected to U9 pin 11. Other details of this section of the report are described below.

- *Logical Pin Name* lists the logical pin names you assign to the symbols by using *Enter*!*Pin* in the Symbol Editor.
- *Symbol Type* is the filename of the gate symbol.
- *Gate Name* is either the name assigned by the system during *Enter*!*Component* or the user–defined name you assign by using *Name*!*Component* in the Schematic Editor.
- *Schematic Sheet* is the filename of the sheet in which the gate is located.
- *Ref Des* is the reference designator you assign to the gate by using *Enter*!*Ref. Des. & Section* in the Schematic Editor.
- *Pin Number* is the physical pin number you assign to the gate by using *Enter*!*Ref. Des. & Section* in the Schematic Editor.

Suspect Nets from netlist1 reports the name of the first netlist (for example, a.nlt), and lists nets that don't match nets in netlist 2. (Nets in netlist 2 that don't match nets in netlist 1 are also listed, but not shown in Figure 6-4.)

- *From sheet/macro* reports the filename of the schematic sheet or third–party macro in which the gates are located.
- *Net Name* is the name assigned by using *Name*!*Net* in the Schematic Editor, or assigned automatically by the system (for example, UN00000033).
- *Logical Pin Name* lists the logical pin names you assign to the symbols by using *Enter*!*Pin* in the Symbol Editor.
- *Gate Type: Name* lists the gate types (base symbol filenames) and either the system–assigned component name (for example, UC00000003) or the user–assigned name (for example, G12).
- *Physical Pin Num* lists the physical pin numbers you assign to the pins by using *Enter*!*Ref. Des. & Section* in the Schematic Editor.
- *Reference Designator* lists the names you assign to the gates by using *Enter*!*Ref. Des. & Section* in the Schematic Editor.

```
==========================================================================================

                 List of Suspect Nets

==========================================================================================

*** NETS FOUND IN BOTH NETLISTS BUT NOT THE SAME ********************
Net Name:  A
- - - - - - -
Pins found in netlist 1 and not in netlist 2
Logical            Gate     Schematic
Pin Name  Symbol Type   Name     Sheet       Ref Des   Pin Number
- - - -  - - - - - -  - - -   - - - - -   - - - -  - - - - - -
INA      cd4011.sym    G12      exboard.sch   U10      1
Pins found in netlist 2 and not in netlist 1
Logical            Gate       Schematic
Pin Name  Symbol Type   Name       Sheet       Ref Des   Pin Number
- - - -  - - - - - -  - - -    - - - - -   - - - -  - - - - - -
OUTY     cd4011.sym    UC00000033  ezboard1.sch  U9       11
Suspect Nets from netlist 1:    a.nlt
From sheet/macro: ezboard.sch
Net      Logical   Gate                 Physical   Reference
Name     Pin Name  Type:Name            Pin Num    Designator
- - -    - - - -   - - - - -            - - - - -  - - - - - -
COUNT_UP  INB      cd4070.sym  :UC00000001    2        U11
        INB       cd4070.sym  :UC00000003    9        U11
        INB       cd4070.sym  :UC00000005    13       U11
        OUTY      cd4011.sym  :UC00000033    11       U9
        INA       cd4011.sym  :UC00000038    5        U9
Total Number of Suspect Nets from sheet/macro :  1
```

Figure 6-4. List of Suspect Nets

List of Spare Gates

In the *List of Spare Gates* section of the report, *Gates from Netlist1* (shown in Figure 6-5) gives the name of the first netlist (for example, a.nlt) and lists the gates that aren't connected to any nets in netlist 1. Other details of this section of the report are described below.

- *From sheet/macro* reports the base filename of the schematic sheet or third–party macro that the gates are in (for example, ezboard).
- *Gate Type:Name* lists the gate types (base symbol filenames) and the component or net names assigned automatically by the system (for example, UC00000002) or the gate types and names you assign by using *Name*! *Component* in the Schematic Editor.

- *Reference Designator* lists the names assigned to the gates by using *Enter* ! *Ref. Des. & Section* in the Schematic Editor (for example, U3).

- *Total Number of Spare Gates from sheet/macro* reports the total number of gates not connected to any nets in this sheet or macro (for example, 2).

Gates from netlist2 reports the name of the second netlist—for example, b.nlt—and lists the gates that aren't connected to nets in netlist 2. The field descriptions are similar to those in *Gates from netlist1* described previously in this section.

```
=========================================================================
           List of Spare Gates
=========================================================================



 Gates from Netlist1:  a.nlt


  From sheet/macro:  ezboard


  Gate Type:Name            Reference Designator
  -------                   ----------

  targ:UC00000002           U3    ( 11    12    13    )
  targ:UC00000001           U3    ( 10     8     9    )


   Total Number of Spare Gates from sheet/macro:  2



 Gates from Netlist2:  b.nlt


  From sheet/macro:  ezboard


  Gate Type:Name
  -------

  targ:UC00000002
  targ:UC00000001


   Total Number of Spare Gates from sheet/macro:  2
```

Figure 6-5. List of Spare Gates

List of Floating Nets

In the *List of Floating Nets* section of the report, *Nets from Netlist1* (shown in Figure 6-6) gives the name of the first netlist (for example, a.nlt) and lists nets that aren't connected to gates in netlist 1. Other details of this section of the report are described below.

- *Net Name* lists the net names of the nets connected to the pins the system assigns automatically (for example, UN00000015) or you assign by using *Name*! *Net* in the Schematic Editor.
- *Total Number of Floating Nets from sheets/macros* reports the total number of nets that aren't connected to any gates in the sheets or macros (for example, 3).

Nets from netlist2 shows the name of the second netlist—for example, b.nlt—and lists nets that aren't connected to any gates in netlist 2. The field descriptions are similar to those in *Nets from netlist1* described previously in this section.

```
==========================================================================
            List of Floating Nets
==========================================================================



 Nets from Netlist1:  a.nlt


  Net Name
  - - - -
  UN00000015
  UN00000014
  UN00000013


   Total Number of Floating Nets from sheets/macros:  3



Nets from Netlist2:  b.nlt


  Net Name
  - - - -
  UN00000015
  UN00000014
  UN00000013


   Total Number of Floating Nets from sheets/macros:  3
```

Figure 6-6. List of Floating Nets

Report Comparing Two PCB Netlists

The netlist comparison report in Figure 6-7 was produced by comparing two PCB netlists. The report first summarizes the comparison results, then lists suspect parts, suspect nets, spare parts, and floating nets, as described below.

- *Number of Parts* reports the total number of parts in each netlist.

- *Number of Nets* reports the total number of nets in each netlist.
- *Number of Suspect Parts* reports the total number of parts that don't match parts in the other netlist.
- *Number of Suspect Nets* reports the total number of nets that don't match nets in the other netlist.
- *Number of Spare Parts* reports the total number of parts that aren't connected to nets in each netlist.

Number of Floating Nets reports the total number of nets that aren't connected to parts in each netlist.

```
%*****************************************************************
%                                              *
%   Program          :   PC*NLC VERSION 8.0   Netlist Comparison    *
%   Date             :   Aug 15 1994                    *
%   Time             :   09:51:29                      *
%   Netlist1         :   a.nlt                       *
%   Netlist2         :   b.pnl                        *
%   Comparison Made  :   WITH Gate Names                        *
%                                              *
%*****************************************************************

                 NLC Report
                 - - - - -

Netlist1: a.pnl                 Netlist2: b.pnl
Number of Parts           12        Number of Parts           12
Number of Nets            52        Number of Nets            53
Number of Suspect Parts    2        Number of Suspect Parts    2
Number of Suspect Nets     2        Number of Suspect Nets     1
Number of Spare Parts      2        Number of Spare Parts      2
Number of Floating Nets    3        Number of Floating Nets    3
```

Figure 6-7. Report Comparing Two PCB Netlists

List of Components With Missing Packaging Information

The *List of Components with Missing Packaging Information* section of the report shown in Figure 6-8 lists components with missing packaging information (for example, 74ls00.prt and 74ls08.prt).

List of Suspect Parts

In the *List of Suspect Parts* section of the report, *Suspect Parts from Netlist1* (shown in Figure 6-9) gives the name of the first netlist (for example, a.pnl) and lists the parts in netlist 1 that don't match other parts in netlist 2 (Figure 6-9). Other details of this section of the report are described below.

- *From board* reports the base filename of the PCB layout that the parts are in (for example, ezboard).
- *Part Type:Name* lists the part types (part base filenames) and reference designators automatically assigned by the system during packaging (for example, 7400:U3) or that you assign by using *Name* ! *Component* in the PCB Editor.
- *Physical Pin Num* lists the physical pin numbers of the part (for example, 1).
- *Physical Pin Name* lists the optional physical pin names you assign to the part by using *Enter* ! *Pin* in the Part Editor.
- *Net Name* lists the net names of the nets connected to the pins assigned automatically by the system (for example, UN00000001) or that you assign by using *Name* ! *Net* in the Schematic Editor (for example, GND).
- *Total Number of Suspect Parts from board* reports the total number of parts in the PCB netlist that don't match other parts in netlist 2 (for example, 2).

Suspect Parts from netlist2 reports the name of the second netlist—for example, b.pnl—and lists the parts in netlist 2 that don't match other parts in netlist 1. The field descriptions are similar to those in *Suspect Parts from netlist1* described previously in this section.

```
==============================================================
    List of Components with Missing Packaging Information:
==============================================================
      74ls00.prt      74ls08.prt


==============================================================

                    List of Suspect Parts

==============================================================

  Suspect Parts from Netlist1:  a.pnl


   From board:  ezboard


   Part          Physical   Physical   Net
   Type:Name        Pin Num    Pin Name   Name
   - - - - -       - - - -    - - - -    - - -

   7400:U3          1              = UN00000001
                 2              = UN00000002
                 3              = UN00000003
                 4              = NET33
                 5              = NET36
                 6              = NET34
                 7              = GND
                 8              = nothing
                 9              = nothing
                 10              = nothing
                 11              = nothing
                 12              = nothing
                 13              = nothing
                 14              = PWR

   7400:U4          1              = UN00000001
                 2              = UN00000002
                 3              = UN00000003
                 4              = NET15
                 5              = NET14
                 6              = Net13
                 7              = GND
                 8              = nothing
                 9              = nothing
                 10              = nothing
                 11              = nothing
                 12              = nothing
                 13              = nothing
                 14              = PWR


     Total Number of Suspect Parts from board:   2
```

Figure 6-8. Missing Packaging Information and Suspect Parts From Netlist1

```
Suspect Parts from Netlist2:  b.pnl

 From board:  ezboard

 Part          Physical  Physical   Net
 Type:Name       Pin Num   Pin Name   Name
 - - - - -      - - - -   - - - -   - - -

 7400:U3          1            = UN00000001
                2            = UN00000002
                3            = UN00000003
                4            = NET33
                5            = NET36
                6            = NET34
                7            = GND
                8            = nothing
                9            = nothing
                10            = nothing
                11            = nothing
                12            = nothing
                13            = NET25
                14            = PWR

 7400:U4          1            = UN00000001
                2            = UN00000002
                3            = UN00000003
                4            = NET15
                5            = NET14
                6            = NET13
                7            = GND
                8            = nothing
                9            = nothing
                10            = nothing
                11            = nothing
                12            = nothing
                13            = NET25
                14            = PWR

   Total Number of Suspect Parts from board:   2
```

Figure 6-9. Suspect Parts From Netlist2

List of Suspect Nets

In the *List of Suspect Nets* section of the report (shown in Figure 6-10) shows the differences when the same nets in each netlist aren’t identical. For example, the report shows the differences in pin connectivity between the net named +IN in netlist 1 and the same net in netlist 2. Other details of this section of the report are described below.

- *Logical Pin Name* lists the logical pin names assigned to the part by using *Enter* ! *Pin* in the Part Editor.
- *Part Type* is the part filename.

- *Ref Des* is the reference designator automatically assigned by the system (for example, U3) or that you assign to the gate by using *Name* ! *Component*.
- *Pin Number* is the physical pin number on the part.

Suspect Nets from netlist1 reports the name of the first netlist (for example, a.pnl) and lists nets that don’t match nets in netlist 2.

- *From board* reports the filename of the PCB layout in which the nets are located.
- *Net Name* is the name automatically assigned by the system or that you assign by using *Name* ! *Net* in the Schematic or PCB Editor.
- *Physical Pin Num* lists the pin numbers of the part.
- *Physical Pin Name* lists the pin names you assign to the part by using *Enter* ! *Pin* in the Part Editor.
- *Part Type:Name* lists the part filename of the part to which the pin belongs and the reference designator or system–assigned component name.

```
========================================================================================
List of Suspect: Nets
========================================================================================
*** NETS FOUND IN BOTH NETLISTS BUT NOT THE SAME *******************
Net Name:  +IN
- - - - - - - -
Pins found in netlist1 and not in netlist1
Logical
Pin Name  Part Type    Ref Des   Pin Number
- - - -  - - - - -    - - - -  - - - - - -
1        res.prt      R6       3
Pins found in netlist2 and not in netlist1
Logical
Pin Name  Part Type    Ref Des   Pin Number
- - - -  - - - - -    - - - -  - - - - - -
2        res.prt      R5       2
Suspect Nets from netlist2:    b.pnl
From board: ezboard.pcb
Net      Physical   Physical   Part
Name      Pin Num    Pin Name   Type:Name
- - -    - - - -   - - - - - - - - - -
POT      2        2         res.prt     :R5
         1        A         tpot.prt    :POT
         2        ARM         tpot.prt    :POT
led+     2        2         led.prt     :DS1
         2        2        led.prt     :DS2
         2        2        led.prt     :DS3
         2        2        led.prt     :DS4
         2        2        led.prt     :DS5
         2        2        led.prt     :DS6
         2        2        led.prt     :DS7
         2        2        led.prt     :DS8
         2        2        led.prt     :DS9
         2        2        led.prt     :DS10
         1        1        RES.prt     :R1
Total Number of Suspect Nets from board :  2
```

Figure 6-10. List of Suspect Nets

List of Spare Parts

In the *List of Spare Parts* section of the report, *Parts from Netlist1* (shown in Figure 6-11) gives the name of the first netlist (for example, a.pnl) and lists parts that aren't connected to any nets in netlist1. Other details of this section of the report are described below.

- *From board* reports the base filename of the PCB layout that the parts are in (for example, ezboard).
- *Part Type:Name* lists the part types (part base filenames) and the reference designators you assign by using *Name* ! *Component* in the PCB Editor (for example, targ:UC00000002).
- *Total Number of Spare Parts from board* reports the total number of parts that aren't connected to any nets in the PCB netlist (for example, 2).

Parts from netlist2 reports the name of the second netlist (for example, b.pnl) and lists the parts that aren't connected to any nets in netlist 2. The field descriptions are similar to those in *Parts from netlist1* described previously in this section.

```
=========================================================================
            List of Spare Parts
=========================================================================


 Parts from Netlist1:  a.pnl

  From board:  EZBOARD

  Part Type:Name
  --------
  targ:UC00000002
  targ:UC00000001

    Total Number of Spare Parts from board:  2



 Parts from Netlist2:  b.pnl

  From board:  ezboard

  Part Type:Name
  --------
  targ:UC00000002
  targ:UC00000001

    Total Number of Spare Parts from board:  2
```

Figure 6-11. List of Spare Parts

List of Floating Nets

In the *List of Floating Nets* section of the report, *Nets from Netlist 1* (shown in Figure 6-12) gives the name of the first netlist (for example, a.pnl) and lists the nets not connected to parts in netlist 1. Other details of this section of the report are described below.

- *Net Name* lists the names of the nets connected to the pins automatically assigned by the system (for example, UN00000005) or that you assign by using *Name* ! *Net* in the Schematic or PCB Editor.
- *Total Number of Floating Nets from board* reports the total number of nets that aren't connected to any parts in the PCB (for example, 2).

Nets from netlist2 reports the name of the second netlist (for example, b.pnl) and lists the nets that aren't connected to any parts in netlist 2. The field descriptions are similar to those in *Nets from netlist1* described previously in this section.

```
==========================================================================
              List of Floating Nets
==========================================================================



 Nets from Netlist1:  a.pnl

  Net Name
  - - - - -
  UN00000005
  UN00000004
  UN00000013

   Total Number of Floating Nets from board:  3




 Nets from Netlist2:  b.pnl

  Net Name
  - - - - -
  UN00000005
  UN00000004
  UN00000013

   Total Number of Floating Nets from board:  3
```

Figure 6-12. List of Floating Nets

Report Comparing a Schematic Netlist and a PCB Netlist

This netlist comparison report shown in Figure 6-13 was produced by comparing a schematic netlist to a PCB netlist. The report first summarizes the comparison results and then lists components with missing packaging information, gates and parts with inconsistent LEQ values, suspect gates, suspect nets, spare gates, and floating nets, as described below.

- *Number of Gates* reports the total number of gates in the schematic netlist.
- *Number of Parts* reports the total number of parts in the PCB netlist.
- *Number of Nets* reports the total number of nets in each netlist.

- *Number of Suspect Gates* reports the total number of gates that don’t match gates in the other netlist.
- *Number of Suspect Nets* reports the total number of nets that don’t match nets in the other netlist.
- *Number of Spare Gates* reports the total number of gates that aren’t connected to nets in each netlist.
- *Number of Floating Nets* reports the total number of nets that aren’t connected to gates in each netlist.

```
%*********************************************************************
%                                              *
%   Program          :  PC*NLC VERSION 8.0   Netlist Comparison  *
%   Date             :  Aug 15 1994                    *
%   Time             :  11:34:17                       *
%   Netlist1         :  a.nlt                          *
%   Netlist2         :  b.pnl                          *
%   Part Reference File  :  t.fil                      *
%                                              *
%*********************************************************************

                 PCNLC Report
                 - - - - - - -

Netlist1: a.nlt                Netlist2: b.pnl

Number of Gates            47        Number of Parts            12
Number of Nets            112        Number of Nets            112
Number of Suspect Gates     3        Number of Suspect Gates     3
Number of Suspect Nets      4        Number of Suspect Nets      4
Number of Spare Gates       2        Number of Spare Gates       2
Number of Floating Nets     3        Number of Floating Nets     3
```

Figure 6-13. Report Comparing a Schematic Netlist and a PCB Netlist

List of Components With Missing Packaging Information

The *List of Components with Missing Packaging Information* section of the report (shown in Figure 6-14) lists the gate and part types with missing packaging information (for example, 74ls32.sym and 74ls08.prt).

List of SCH Gates and PCB Parts With Inconsistent Pin LEQ Values

The *List of SCH Gates and PCB Parts with Inconsistent Pin LEQ Values* section of the report (shown in Figure 6-14) lists the gate and part types with inconsistent pin LEQ values. When no corresponding symbol type is found in the schematic database for a part type, it’s shown as a dashed line. For example, no corresponding symbol type was found for part type 74ls04.prt; *Netlist Comparison* therefore assumed the pin LEQ values were inconsistent.

List of Suspect Gates

In the *List of Suspect Gates* section of the report, *Suspect Gates from Netlist1* (shown in Figure 6-14) gives the name of the first netlist (for example, a.nlt) and lists the gates in netlist 1 that don't match other gates in netlist 2. In this example, netlist1 is from a schematic sheet. Other details of this section of the report are described below.

- *From sheet/macro* reports the base filename of the schematic sheet or third–party macro in which the gates are located (for example, ezboard).
- *Gate Type:Name* lists the gate types (gate base symbol filenames) and the component or net names automatically assigned by the system (for example, nand2:A10) or that you assign by using *Name*! *Component* in the Schematic Editor.
- *Logical Pin Name* lists the logical pin names you assign to the symbols by using *Enter*! *Pin* in the Symbol Editor (for example, INA).
- *Net Name* lists the net names of the nets connected to the pins automatically assigned by the system (for example, UN00000001) or that you assign by using *Name*! *Net* in the Schematic Editor.
- *Physical Pin Num* lists the pin numbers you assign to the gates by using *Enter*! *Ref. Des. & Section* in the Schematic Editor (for example, 1).
- *Reference Designator* lists the names you assign to the gates by using *Enter*! *Ref. Des. & Section* in the Schematic Editor (for example, U1).
- *Total Number of Suspect Gates from sheet/macro* reports the total number of gates (in this sheet or macro) that don't match other gates in netlist 2 (for example, 3).

```
========================================================================
    List of Components with Missing Packaging Information:
========================================================================
      74ls32.sym      74hs00.sym
      74ls00.prt      74ls08.prt



========================================================================
   List of SCH Gates and PCB Parts with Inconsistent Pin LEQ Values:
========================================================================
      Symbol Type      Part Type
      ------      -----
      74ls00.sym      74ls00.prt
      74ls31.sym      74ls31.prt
      ------      74ls04.prt
      inv.sym         74ls31.prt
      nand.sym        74ls31.prt


========================================================================
              List of Suspect Gates
========================================================================
 Suspect Gates from Netlist1:  a.nlt

  From sheet/marco:  ezboard

  Gate          Logical    Net       Physical   Reference
  Type:Name        Pin Name   Name       Pin Num    Designator
  -----        ----   ---      ----   -----
  nand2:A10        INA      = UN00000001    1      U1
           INB      = UN00000002    2
           OUTY     = QA1           3

  nand2:A11        INA      = UN00000003    4      U1
           INB      = UN00000004    5
           OUTY     = QA2           6

  nand2:A12        INA      = UN00000005    10     U1
           INB      = UN00000006    9
           OUTY     = QA3           8

   Total Number of Suspect Gates from sheet/macro:   3


 Suspect Gates from Netlist2:  b.pnl

  From board:  EZBOARD

  Part          Logical    Net       Physical   Reference
  Type:Name        Pin Name   Name       Pin Num    Designator
  -----        ----   ---      ----   ------
  7400:U11         INA      = UN00000001    1      U11
           INB      = UN00000002    2
           OUTY     = QA1           3

  7400:U11         INA      = UN00000003    4      U11
           INB      = UN00000004    5
           OUTY     = QA2           6

  7400:U11         INA      = UN00000005    10     U11
           INB      = UN00000006    9
           OUTY     = QA3           8

   Total Number of Suspect Gates from board:   3
```

Figure 6-14. Missing Packaging Information, Inconsistent LEQ Values, and Suspect Gates

Suspect Gates from netlist2 reports the name of the second netlist, a PCB netlist (for example, b.pnl) and lists the gates in netlist 2 that don’t match other gates in netlist 1.

- *From board* reports the base filename of the PCB layout in which the parts are located (for example, ezboard).

- *Part Type:Name* lists the gates types that make up the part types (base gate filenames) and the reference designators automatically assigned by the system during packaging (for example, 7400:U11) or that you assign by using *Name*!*Component* in the Schematic or PCB Editor.
- *Logical Pin Name* lists the logical pin names you assign to the schematic symbols by using *Enter*!*Pin* in the Symbol Editor (for example, INA).
- *Net Name* lists the net names of the nets connected to the pins automatically assigned by the system (for example, UN00000001) or that you assign by using *Name*!*Net* in the Schematic Editor.
- *Physical Pin Num* lists the physical pin numbers of the part (for example, 1).
- *Reference Designator* lists the names automatically assigned to the parts by the system during packaging (for example, U11) or that you assign by using *Name*!*Component* in the PCB Editor.
- *Total Number of Suspect Gates from board* reports the total number of gates in the PCB that don't match other gates in netlist 1 (for example, 3).

List of Suspect Nets

The *List of Suspect Nets* section of the report (shown in Figure 6-15) gives the differences when the same nets in each netlist aren't identical. For example, the report shows that the net named A in netlist 1 includes a pin that isn't part of net A in netlist 2. Other details of this section of the report are described below.

- *Logical Pin Name* lists the logical pin names you assign to the symbols by using *Enter*!*Pin* in the Symbol Editor.
- *Symbol Type* is the symbol filename for the gate.
- *Gate Name* is the gate name automatically assigned by the system or that you assign by using *Name*!*Component* in the Schematic Editor.
- *Schematic Sheet* is the sheet filename in which the gate is located.

- *Ref Des* is the reference designator automatically assigned to the gate by the system during packaging or that you assign by using either *Enter*!*Ref. Des. & Section* in the Schematic Editor for schematic symbols or *Name*!*Component* in the PCB Editor for PCB parts.

- *Pin Number* is the physical pin number you assign to the pins by using either *Enter*!*Ref. Des. & Section* in the Schematic Editor for schematic symbols or *Enter*!*Pin* in the Part Editor for PCB parts.

Suspect Nets from netlist1 reports the name of the first netlist (for example, a.nlt) and lists nets that don’t match nets in netlist 2.

- *From sheet/macro* reports the filename of the schematic sheet or third–party macro in which the gates are located.

- *Net Name* is the name automatically assigned by the system or that you assign by using *Name*!*Net* in the Schematic Editor.

- *Logical Pin Name* lists the logical pin names you assign to the symbols by using *Enter*!*Pin* in the Symbol Editor.

- *Gate Name* lists the gate types (base symbol filenames) and the name automatically assigned to the gate by the system or that you assign by using *Name*!*Component* in the Schematic Editor.

- *Physical Pin Num* lists the pin numbers you assign to the pins by using *Enter*!*Ref. Des. & Section* in the Schematic Editor.

- *Reference Designator* lists the names you assign to the gates by using *Enter*!*Ref. Des. & Section* in the Schematic Editor.

```
=======================================================================================
                                    List of Suspect Nets
=======================================================================================

*** NETS FOUND IN BOTH NETLISTS BUT NOT THE SAME ********************

Net Name:  A
- - - - -- - - - -

    Pins found in netlist 1 and not in netlist 2

        Logical          Gate     Schematic
        Pin Name  Symbol Type  Name     Sheet     Ref Des  Pin Number
        - - - -  - - - - - -  - - -     - - - - -   - - - -  - - - - -- - -  - - -    - - - - -   - - - -  - - - -
        OUTY    cd4011.sym  UC00000033  ezboard.sch  U9     11

Net Name:  +IN
- - - - -- - - - - - - -

    Pins found in netlist 2 and not in netlist 1

        Logical
        Pin Name  Part Type   Ref Des  Pin Number
        - - - -  - - - - -   - - - -  - - - - -- - - -  - -- -- -- - -
        2       res.prt     R5     2

Suspect Nets from netlist 1:   a.nlt

    From sheet/macro: ezboard.sch
    Net     Logical   Part              Physical  Reference
    Name     Pin Name  Type              Pin Num   Designator
    - - -    - - - -  - - -             - - - - -  - - - - - -- - -   - - - -  - - -
    POT     A       tpot.sym   :UC00000046   1       POT
             ARM      tpot.sym   :UC00000046   2       POT
             2        res.sym    :UC00000054   2       R5
    led+    A       led.sym    :UC00000017   2       DS1
            A       led.sym    :UC00000018   2       DS2
            A       led.sym    :UC00000019   2       DS3
            A       led.sym    :UC00000020   2       DS4
            A       led.sym    :UC00000021   2       DS5
```

Figure 6-15. List of Suspect Nets

```
          A     led.sym   :UC00000022   2     DS6
          A     led.sym   :UC00000023   2     DS7
          A     led.sym   :UC00000024   2     DS8
          A     led.sym   :UC00000025   2     DS9
          A     led.sym   :UC00000026   2     DS10
          1     res.sym   :UC00000028   1     R1
               Total Number of Suspect Nets from sheet/macro :  2

  Suspect Nets from netlist 2:  b.pnl
      From board: ezboard.pcb

      Net    Logical   Part              Physical   Reference
      Name    Pin Name  Type               Pin Num   Designator
      ---   ----  -----         ----  ---   ----  --------
      A&F     R       cd4013.prt  :U12      4      U12
              R       cd4013.prt  :U12      10     U12
           OUTY      cd4001.prt  :U1       11     U1
COUNT_UP  INB       cd4070.prt  :U11      2      U11
          INB       cd4070.prt  :U11      9      U11
          INB       cd4070.prt  :U11      13     U11
          INA       cd4011.prt  :U9       5      U9
          OUTY      cd4011.prt  :U9       11     U9
             Total Number of Suspect Nets from board :  2
```

Figure 6-15. List of Suspect Nets (cont'd)

Suspect Nets from netlist2 gives the name of netlist 2 (not shown in the example) and lists nets that don't match any nets in netlist 1.

- *From board* reports the name of the board in which the parts reside.
- *Net Name* is the name automatically assigned by the system or that you assign by using *Name* ! *Net* in the Schematic Editor.
- *Logical Pin Name* lists the logical pin names you assign to the PCB part by using *Enter* ! *Pin* in the Part Editor.
- *Part Type* lists the part filename of the part to which the pin belongs.
- *Physical Pin Num* lists the pin numbers of the part.
- *Reference Designator* lists the names automatically assigned to the parts by the system during packaging or that you assign by using *Name* ! *Component* in the Schematic or PCB Editor.

List of Spare Gates

In the *List of Spare Gates* section of the report, *Gates from Netlist 1* (shown in Figure 6-16) gives the name of the first netlist (for example, a.nlt) and lists the gates that aren't connected to any nets in netlist 1. Other details of this section of the report are described below.

- *From sheet/macro* reports the name of the sheet or macro in which the gates are located (for example, ezboard).
- *Gate Type:Name* lists the gate types (base symbol filenames) and the component or net names automatically assigned by the system (for example, targ:UC00000002) or that you assign by using *Name* ! *Component* in the Schematic Editor.
- *Reference Designator* lists the names you assign to the gates by using *Enter* ! *Ref. Des. & Section* in the Schematic Editor (for example, U3).
- *Total Number of Spare Gates from sheet/macro* reports the total number of gates that aren't connected to nets in this sheet or macro (for example, 2).

Gates from netlist 2 gives the name of the second netlist (for example, b.pnl) and lists the gates that aren't connected to any nets in netlist 2.

- *From board* reports the name of the board that the gates are in (for example, ezboard).
- *Part Type:Name* lists the part filenames and the reference designator automatically assigned by the system during packaging (for example, ptarg:U9) or that you assign by using *Enter* ! *Ref. Des. & Section* in the Schematic Editor.
- *Reference Designator* lists the names automatically assigned to the parts by the system during packaging (for example, U9) or that you assign by using *Enter* ! *Ref. Des. & Section* in the Schematic or PCB Editor.
- *Total Number of Spare Gates from board* reports the total number of gates that aren't connected to any nets in this board (for example, 2).

```
========================================================================
           List of Spare Gates
========================================================================



 Gates from Netlist1:  a.nlt


  From sheet/macro:  ezboard


  Gate Type:Name              Reference Designator
  - - - - - - - -             - - - - - - - - - -

  targ:UC00000002             U3    ( 11    12    13    )
  targ:UC00000001             U3    ( 10    8     9     )


   Total Number of Spare Gates from sheet/marco:  2



 Gates from Netlist2:  b.pnl


  From board:  ezboard


  Part Type:Name          Reference Designator
  - - - - - - - -         - - - - - - - - - -

  ptarg:U9                U9
  ptarg:U9                U9


   Total Number of Spare Gates from board:  2
```

Figure 6-16. List of Spare Gates

List of Floating Nets

In the *List of Floating Nets* section of the report, *Nets from netlist1* (shown in Figure 6-17) gives the name of the first netlist (for example, a.nlt) and lists the nets that aren’t connected to gates in netlist 1. Other details of this section of the report are described below.

- *Net Name* lists the net names of the nets connected to the pins automatically assigned by the system (for example, UN00000035) or that you assign by using *Name* ! *Net* in the Schematic Editor.

- *Total Number of Floating Nets from sheets/macros* reports the total number of nets that aren’t connected to any gates in the sheets or macros (for example, 3).

```
============================================================================
              List of Floating Nets
============================================================================


 Nets from Netlist1:  a.xnl

  Net Name
  - - - - -
  UN00000035
  UN00000034
  UN00000033


   Total Number of Floating Nets from sheets/macros:  3



 Nets from Netlist2:  b.pnl

  Net Name
  - - - - -
  UN00000035
  UN00000034
  UN00000033


   Total Number of Floating Nets from board:  3
```

Figure 6-17. List of Floating Nets

List of Components With COMPARE=MECH Attribute Value

In the *List of Components with COMPARE=MECH Attribute Value* section of the report, *Gates from PCB Netlist* (shown in Figure 6-18) gives the name of the packaged PCB netlist (for example, b.pnl) and lists the components having the COMPARE=MECH attribute value. Other details of this section of the report are described below.

- *From board* reports the filename of the PCB layout in which the components are located (for example, ezboard).
- *Part Type:Name* lists the part filenames and the reference designators you assign by using *Name* ! *Component* in the PCB Editor (for example, 7400.prt:UC00000002).
- *Reference Designator* lists the names assigned to the parts automatically by the system (for example, UC00000002) or that

you assign by using *Name* ! *Component* in the PCB Editor (for example, U3).

- *Total Number of Spare Gates from board* reports the total number of gates with the COMPARE=MECH attribute value in this board (for example, 4).

```
========================================================================
            List of Components with COMPARE=MECH Attribute Value
========================================================================

 Gates from PCB Netlist:  b.pnl

    From board:  ezboard

    Part Type:Name                  Reference Designator
    --------                        -----------

   7400.prt  :UC00000002     UC00000002   13       11       )
   7400.prt  :UC00000002     UC00000002  ( 9       10       8        )
   7400.prt  :UC00000002     UC00000002  ( 4       5        6
   7400.prt  :UC00000002     UC00000002  ( 1       2        3

   Total Number of Spare Gates from board:  4

========================================================================
                        List of System Named Parts
========================================================================

  From board:  ezboard

  Part Type:Name
  --------

   7400.prt  :UC00000002     UC00000002
   7400.prt  :UC00000002     UC00000001
   7400.prt  :UC00000002     UC00000002

   Total Number of Parts from board:  3
```

Figure 6-18. Components With COMPARE=MECH Attribute and System-Named Parts

List of System–Named Parts

The *List of System–Named Parts* section of the report (also shown in Figure 6-18) lists parts that were automatically named by the system.

- *From Board* reports the filename of the PCB layout in which the components are located (for example, ezboard).
- *Part Type: Name* lists the part filenames and the reference designators automatically assigned by the system (for example,

7400.prt:UC00000002) or that you assign by using the PCB Editor.

- *Total Number of Parts from board* reports the total number of parts with system–assigned names parts in this PCB layout (for example, 3).

Using the Command Line Mode

You can run *Netlist Comparison* at any time without using the P–CAD graphical interface by entering a command line at the DOS prompt.

You can specify the netlists to compare, cross–reference file (if used), or any report format options when comparing netlists from the command line.

You must have at least one of these input files before you can compare netlists from the command line:

- an extracted netlist from a single schematic sheet (.nlt)
- an expanded netlist from a multisheet schematic (.xnl)
- an extracted netlist from a packaged PCB (.pnl)
- an annotated schematic netlist from packaging and using the *Engineering Change Order (ECO)* tool (.bnl)

For more information on creating these files from a command line format, see the section on packaging schematics in the *Schematic Tools* manual.

To run *Netlist Comparison* from the command line

1. Go to the DOS prompt.
2. Use the following command line:

   pcnlc [options] <netlist1> <netlist2>

   where

   pcnlc initiates the program execution.

   options is one or more of the options listed below that correspond to the configuration options. For some options, a filename is required.

   -*h* prints the help message on the screen. The -*h* is optional.

-*n* instructs the program to use gate/part name checking in comparison.

-*o reportfile* specifies the output report file. If this option is not entered, the default report file name is netlist1.nlc.

netlist1 is the name of the first input netlist file and is required.

netlist2 is the name of the second input netlist file and is required.

An example of a command line entry using *pcnlc* is

```
pcnlc  -n -o a.nlc a.nlt b.nlt
```

In this example, *pcnlc* uses the component and net name checking option in the comparison and specifies a.nlc as the output report filename. The comparison is made between netlist1, a.nlt and netlist2, b.nlt. Status and any error messages are written to the pcnlc.log file. When the processing is complete, the system returns to the DOS prompt.

Creating a Batch File

You can run several comparisons consecutively by creating a batch file that contains command line instructions for each comparison. Use a text editor to create the ASCII batch file. Each line of the file should contain a separate set of command line instructions. If you run multiple comparisons using the same input netlist, be sure to specify unique output report filenames.

You must use .bat as a filename extension for your batch file. The following is an example of a batch file for comparing netlists.

pcnlc sch1.nlt sch2.nlt –n
pcnlc pcb1.pnl pcb2.pnl –o *filename*
pcnlc sch3.bnl pcb3.pnl

To run the batch file, enter the filename at the DOS prompt.

The program runs as many times as the number of *pcnlc* command lines listed in the batch file. When processing is complete, the system returns to the DOS prompt.

Annotating Engineering Changes 7

You use the *Engineering Change Order (ECO)* tool to update a schematic database or a PCB database so the databases reflect the latest engineering changes.

ECO can forward–annotate a PCB database by transferring logic data from a schematic database. *ECO* can also back–annotate a schematic database by transferring packaging changes from a PCB database.

Both forward–annotation and back–annotation help you to keep the schematic database and the PCB database consistent. *ECO* updates the databases so that they're logically and electrically equivalent.

This chapter contains information about the following:

- forward–annotating and back–annotating a database
- analyzing the differences between a schematic and a PCB database
- reviewing the *Update* command file (.upd)
- interpreting the *ECO* report

You can use *ECO* to make the changes listed in Table 7-1.

Table 7-1. Database Changes After Running ECO

Forward–Annotation	***Back–Annotation***
Adds parts, nets, and pins designators to the PCB database	Back–annotates reference to gates of the schematic databases
Highlights parts that should be the deleted from the PCB database (*ECO* doesn't delete the parts.)	Swaps gates and components in schematic database
Names nets in the PCB database	Names nets in the schematic database
Deletes nets and uncommits pins from the PCB database	—
Adds and updates attributes to the PCB database (optional)	*Update*s existing attributes to the schematic database (optional)
Creates a new $*ECO* layer that contains symbols representing the database changes	—
Reports parts and nets that don't match in the two databases	Reports parts and nets that don't match in the two databases

Note: *ECO* doesn't make topological changes (deleting gates, rewiring nets, and adding symbols) to schematic databases when it's performing back–annotation. However, *ECO* does identify and report parts and nets that need to be modified.

When to Run the *Engineering Change Order* Tool

You run *ECO* on your PCB design when you've made changes to your schematic or PCB databases after you've used the Schematic Packager. You make the required changes to either the schematic database or the PCB database, then run *ECO* to compare and analyze the two databases and make the required changes.

To run *ECO*, you need a packaged PCB database (*filename*.pcb) and the schematic database (*filename*.sch) you used to package the PCB. If you packaged the schematic using a cross–reference file (*filename*.fil), you also need that file in your current design directory. You need to enter the cross–reference filename in the Design Manager. See Chapter 2, "Maintaining Design Files."

Note: If you add parts when you modify a schematic, you need to put the new part files in the current design directory before you run *ECO* to forward–annotate the PCB database.

When Not to Run the *Engineering Change Order* Tool

Because *ECO* operates across the entire P–CAD design system, the program makes certain assumptions about the consistency of libraries and the order in which engineering changes are applied to the schematic and PCB databases. For these reasons, it's important that you clearly understand when not to use *ECO*.

Note: You must use the Schematic Packager to create the PCB database if you want to use *ECO* to update either the schematic or the PCB database.

Don't use *ECO* under the following circumstances:

- During the initial packaging of the schematic:

  —The P–CAD design process is most efficient when you do your initial packaging using the Schematic Packager. Don't use *ECO* for initial packaging of the design. Always use the Schematic Packager for the following reasons:

—Using the Schematic Packager is faster and more efficient early in the design process. It provides detailed, comprehensive reports and messages that help you detect any errors that may occur during the initial design process.

—Resolving errors is less time–consuming when you use the Schematic Packager. The packaging tool reports and identifies each problem so you can fix it, whereas *ECO* is used to compare the schematic to the PCB.

- To make logic changes from the PCB to the schematic

  Schematics are the basis of the PCB design. Therefore, you need to make all logic changes at the schematic level. The only changes you can make at the PCB level are resequencing reference designators and swapping gates and components.

- When engineering changes are out of step:

  After you create the schematic and PCB databases for a design, you must maintain a certain discipline to ensure that engineering changes are made consistently. It's easy to make changes to the schematic and the PCB independently. However, this practice can cause the engi– neering changes to get out of step, so that changes are pending in both the schematic and the PCB at the same time.

  For example, if a designer uses a spare 74ls00 part as an inverter at the same time the engineer is using it to implement additional logic, two conflicting changes are pending in the system.

  To avoid this type of problem, observe the following guidelines:

  —Make changes to only one database at a time.

  —If a design gets out of step, compare netlists to determine differences between the schematic and the PCB. You can manually update either the schematic or the PCB to bring your design to the state where only one set of changes is pending. After you complete the changes in one database, run *ECO* to update the other database.

- When symbol and part libraries used in the design are inconsistent.

  When you're working with existing designs, it's common for packaging definition inconsistencies to exist between symbols and parts. If so, you need to resolve the inconsistencies before you run *ECO*.

How to Run the *Engineering Change Order* Tool

The Engineering Change Order tool (*ECO*) consists of three options:

1. *Compare* - compares a PCB database with its corresponding schematic database and analyzes the differences between the two. *Compare* creates an update command file and a Compare/Analysis report.

2. *Update* - reads the update command file and makes the changes to the schematic or PCB databases.

3. *PC–BACK* -uses the PCB swap report file data to update the reference designators in the schematic database. *PC–BACK* is used only during back annotation and then only if you have swapped gates or pins in the PCB layout.

When you perform forward annotation, you run *Compare* to generate the update command file, then run *Update* to actually update the PCB database. You can run both *Compare* and *Update* at the same time, or run each option separately. Running *Compare* by itself allows you to check the Compare/Analysis Report and edit the update command file, if necessary, before running *Update* to update the PCB database.

When you perform back annotation, the process is the same as for forward annotation except that you have the additonal option of running *PC–BACK*. You run *PC–BACK* if you have swapped any gates or pins in the PCB layout. *PC–BACK* updates the schematic with the swap information prior to running *Compare*.

What Happens When You Run *Compare*

This section explains the comparison and analysis process that takes place when you run *Compare*. You can also run *Update* and *PC–BACK* when you run *Compare*. Refer to What Happens When You Run *Update* and What Happens When You Run *PC–BACK* in this chapter.

Compare attempts to identify changes in

- logic
- packaging
- net names
- attributes

Compare first copies the PCB database to a file with the same filename as the original and changes the extension to .pbk.

During forward–annotation, *Compare* compares logic changes in the schematic to the PCB database using packaging information as a basis. During back–annotation, *Compare* assumes the board logic is correct and updates packaging changes to the schematic.

Compare compares a schematic netlist and a PCB netlist. The items in each netlist are either matched or unmatched. Matched items have corresponding data in both the schematic and PCB netlists. For example, matched gates have the following corresponding data:

- In forward–annotation, two gates match if they're the same component type, have the same nets connecting them, and have the same reference designators.
- In back–annotation, two gates match if they're the same component type and have the same nets connecting them.

If you run *PC–BACK* with *Back–Annotation*, reference designators will be assigned according to information in a swap report file, *filename.*rpt, created when using a swap command in the PCB Editor

Matched nets have the following corresponding data:

- In forward–annotation, two nets match if they have the same number of pins and all corresponding pins connect to the same gate type and reference designator.
- In back–annotation, two nets match if they have the same number of pins, all corresponding pins connect to the same gate type, and the pin LEQs are consistent.

If you have components such as bypass capacitors which typically all have the same number of pins connected to the name nets (such as +5v and GND), you have to run *PC–BACK* to update any reference designators that were changed on these components during the PCB layout. *PC–BACK* uses the swap report, *filename*.rpt, created during swap or resequence activity in the PCB Editor, to update the corresponding components in the Schematic.

Unmatched items in the database are gates and nets that appear in one netlist but not in the other. If *Compare* finds unmatched items, it reports them.

Net Names, Attributes, Part Names, and Critical Path Information

You can assign net names in the PCB Editor or the Schematic Editor using *Name* ! *Net.* If you don't assign a net name in the Schematic Editor, the system automatically assigns a name for you. System net names have the following format:

UN*xxxxyyyy*

where *xxxx* is the sheet number and *yyyy* is the net number.

If two matched nets have different names and you fill the *Update* Net Names check box, *Compare* updates the user–assigned net names.

Note: *Compare* doesn't update the system–assigned net names in the schematic database (when you're running back–annotation) or in the PCB database (when you're running forward–annotation).

You can specify attribute keywords in the Schematic Packager to be carried over to the PCB database from the schematic database. During forward–annotation or back–annotation, if the attributes don't match in the two databases, *Compare* reports the differences. If you changed attributes in either database, you can specify the attribute keywords you want to apply in the list box in the *Compare* screen.

When you perform forward–annotation and a SYSTEM command appears in the update file as SYSTEM PCAD, *Compare* removes all critical path and group information from the PCB and replaces it with critical path and group information from the schematic. If the system name isn't PCAD, or if no SYSTEM command was found, *Compare* doesn't modify the critical path or group information on the PCB. Refer to the Update Commands section later in this chapter for an explanation of the SYSTEM command.

Nonelectrical Components

Nonelectrical components in the PCB database include graphic entities such as title blocks, datum points, and optical targets; and physical parts such as card ejectors, nuts, bolts, and screws. Because these components don't have corresponding electrical symbols in the schematic and don't participate in the logic of the design, don't include them in the comparison and analysis process.

To prevent nonelectrical components from being included in the comparison, assign a component ID type of 0 to the part, or use attribute COMPARE=MECH. *Compare* ignores parts with component ID types of 0 or parts with the COMPARE=MECH attribute during the comparison and analysis process. *Compare* reports them in the .eco report file. *Compare* ignores, but still reports, parts specified as jumpers using *Enter* ! *Jumper* in the Part Editor.

Analyzing Data for Forward–Annotation

For forward–annotation, *Compare* determines logic changes made in the schematic database by comparing the schematic database to the PCB database. *Compare* treats any packaging differences (such as a 7400 gate that was moved from U1/A to U1/B in the schematic) as though the original gate (U1/A) in the PCB is to be deleted, and a new gate (U1/B) is to be added to the PCB. If gate types were changed (such as a 7400 that was changed to a 74ls00), *Compare* marks the original gate in the PCB and adds the new gate to the PCB.

Compare determines how to modify the PCB to match the schematic by analyzing and processing the unmatched nets in the netlists first. After all the nets are corrected, the remaining unmatched components become spares. When the schematic database has spare components, *Compare* adds them to the PCB database.

If the PCB has spare components, or if some components become spares through logic changes to the schematic, *Compare* doesn't delete them. Instead, the program highlights those parts by putting a box around them. You must manually delete them in the PCB database using the PCB Editor, or replace the *HIGHLIGHT PART* command with a *DELETE PART* command in the *Update* command file (see Understanding the *Update* Command File in this chapter).

Compare completes the following steps to determine mismatches between nets in the PCB and nets in the schematic netlist:

1. It first locates the nets in the PCB database and the schematic databases that match exactly. These matched nets aren't further analyzed.

2. *Compare* then begins to analyze the unmatched nets from the schematic and PCB databases. It determines which nets in the

PCB need to be modified to match the nets in the schematic, as follows:

—It finds the two nets with matching net names.

—For the remaining nets, it finds the two nets with the most connecting pins in common. If two nets have the same number of connecting pins in common, the two nets with common source pins are matched.

3. If the schematic database has remaining nets that don't match a net in the PCB, they're added to the PCB database. If the PCB database has remaining nets that don't match a net in the schematic, they're deleted from the PCB database.

When *Compare* finds two matching nets using the above steps, it examines and compares the pins in the schematic net to find the corresponding pin in the PCB net. If the pin is in the schematic net but not the PCB net, *Compare* adds a command to the *Update* command file to add the pin to the PCB net. If the pin is in the PCB net but not the schematic net, *Compare* adds a command to the *Update* command file to delete the pin from the PCB net that the program can't match in the schematic net.

Analyzing Data for Back–Annotation

For back–annotation, *Compare* compares the logic of the schematic database and the PCB database. *Compare* looks for packaging changes that were made in the PCB database.

Note: Use the *Package Schematic* tool in the Schematic Tools module to package a PCB database from your schematic design. This ensures that reference designators will be automatically assigned if they were not assigned during schematic layout. When you use the *Package Schematic* tool, be sure to enable the Back–Annotation option, so that any reference designators assigned by the system during packaging can be back–annotated to the schematic files.

Compare assumes that the logic in the schematic and the PCB databases is the same. If it's not, gates and nets that aren't the same are reported as unmatched items. Only the matching gates are used in the packaging information comparison. If the packaging data differs, the gate in the schematic database is changed to match the one in the PCB database.

In back–annotation, two gates match if they're the same component type and have the same nets connecting them. Two nets match if they have the same number of pins, all corresponding pins connect to the same gate type, and the pin LEQs are consistent. Using these rules, *Compare* views components such as bypass capacitors as matching. But often these components are resequenced at the end of the layout process, and in the designer's view, they are no longer the same component, since they now have different reference designators.

When you use *Package Schematic* to produce a PCB database and all the PCB components have been asssigned reference designators, you can often improve upon the packaging assignments by using a PCB Editor swap command. The swap report file (*filename*.rpt) is produced automatically by the PCB Editor. The swap report file keeps track of all swap activity during the editor session. If a swap report exists in the current design directory you can choose to append the report.

When you run *PC–BACK* during back–annotation, *ECO* uses the swap report created by the PCB Editor to resequence all components in the schematic, based on the resequence instructions in the report. This works very efficiently, as long as all the other criteria for matching gates and nets are met.

If you swap pins, gates, or components or resequence reference designators during multiple sessions in the PCB Editor, when you exit the editor, you can run *Compare* and *PC–BACK* right away to update the changes to your schematic using the swap report instructions. Or you can append the report each time you use the PCB Editor and run *Compare* and *PC–BACK* at the end of your layout process to update the schematic all at once.

It is recommended that you run *Compare* and *PC–BACK* as soon and as often as you can to avoid getting the schematic too far out of step with the PCB. When you run *PC–BACK*, you must also run *Update*, in order for the changes to be made in the schematic.

What Happens When You Run *Update*

This section explains what happens if you fill the Run *Update* check box when you run *ECO*. If you don't run *Update*, *ECO* doesn't process the *Update* command file and doesn't make changes to either the schematic or the PCB database.

The following steps describe how the system processes the update command file, *filename*.upd, when you run *Update*.

1. *Update* executes the commands in the update file one by one, then modifies each line in the command file by inserting a percent sign in front of the command just executed. The percent sign converts each command line to a comment.

If *Update* encounters an error while it's executing a command, it stops executing the remaining commands until it encounters a successful *LOAD* command. However, *Update* checks the remaining commands to be applied to that database for syntax and semantic errors. Execution stops if *Update* encounters syntax or semantic errors or can't find pertinent data in the database.

The *LOAD* command doesn't automatically save any previously loaded database. A *Save* command is required to save the database.

2. At the end of the *Update* command file, *Update* tries to save the last database if it was modified but not saved.

3. After *Update* processes all commands, the same commands are echoed to the *Update* log file in the output report file (*filename*.eco) along with any warnings and error messages. (Make sure you check the .eco file for any errors.) *Update* then deletes the command file (*filename*.upd).

What Happens When You Run *PC–BACK*

You can only run *PC–BACK* during the back–annotation process. If you don't run *PC–BACK*, certain component reference designators may not get updated in the schematic during back–annotation.

The following steps deacribe how *ECO* processes the *PC–BACK* instruction file and the PCB swap report.

1. *ECO* runs the *Package Schematic* tool again to regenerate the schematic netlists. A *PC–BACK* instruction file, *filename*.bck, is created. This file contains instructions to rename the components in the schematic the same as in the PCB.

2. *ECO* then takes the swap report file created by the PCB Editor, *filename*.rpt, and using the .bck instruction file, creates an update instruction file that can be read in Update format, *filename*.bka. *ECO* processes the update file and, based on the instructions in the .bka file, creates a new schematic to match the PCB.

3. After *ECO* processes the commands in the update file, it regenerates an expanded schematic node list, *filename*.xnl, and compares it to the netlist for the PCB, *filename*.pnl. A comparison is made of these two netlists, and the Compare/Analyze phase is run.

4. At the end of the comparison and analysis, two reports are created, *filename*.eco and *filename*.out. The .eco file is the report of the Compare/Analyze phase, and the .out file is the report of all component name changes made as a result of running *PC–BACK*.

You must have a swap report file (*filename*.rpt) in order to run *PC–BACK*. If there were any errors found during execution of *PC–BACK*, including syntax and semantic errors, they are recorded in pcad.log. If errors were found, the components involved are listed in the pcad.log file.

You don't need to run *Update* when running *PC–BACK* unless you want to run the Compare/Analyze phase of the back–annotation process.

Opening the Engineering Change Order Screen

You open the Engineering Change Order screen from the Design Manager screen.

To open the Engineering Change Order screen

- Select *Engineering Change Order.* You'll see the *ECO* screen shown in Figure 7-1.

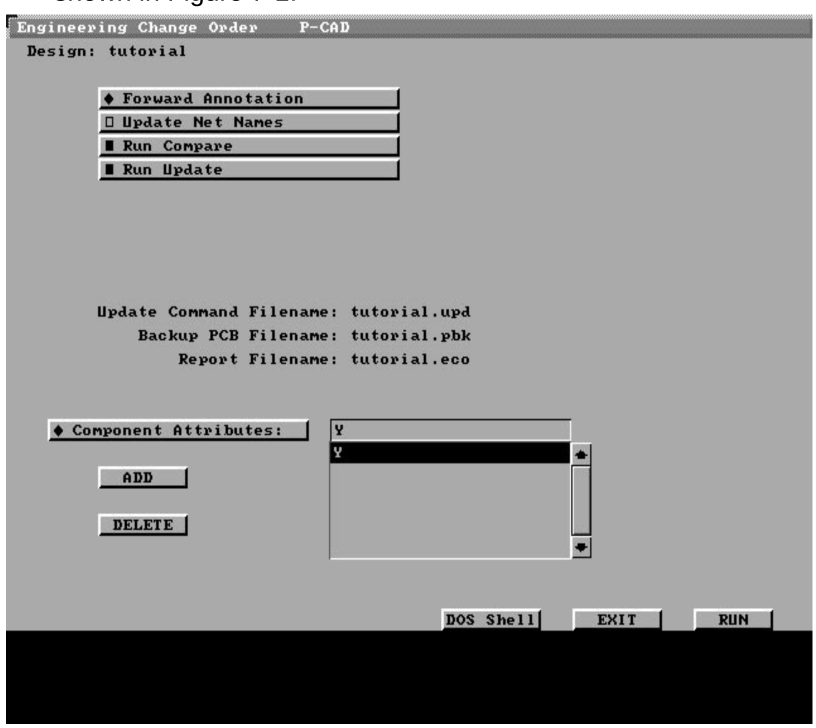

Figure 7-1. Engineering Change Order Screen

Annotating a Database

You run *ECO* to annotate a schematic or PCB database when changes are made to one or the other database. Annotation is information that shows the differences that exist between a schematic and a PCB database. If you made changes to the schematic database and want to annotate the PCB database, you need to use forward–annotation. If you made changes to the PCB database and want to annotate the schematic database, you need to use back–annotation.

You can run *ECO* with or without updating the target database. If you update the database, *ECO* notes the differences in the *ECO* report and makes the indicated changes. If you don't update the database, *ECO* simply notes the differences but doesn't change either database. For more information, refer to "What Happens When You Run *Update*" in this chapter.

You can also forward–annotate or back–annotate net names in the PCB database or schematic database to make the names consistent between the two databases. However, you need to name any nets you've added so *ECO* can update the net names.

If two matched nets have different names and you fill the Update Net Names check box, *ECO* applies the user–assigned net names. It doesn't apply the system–assigned net names in the schematic database (when you're running back–annotation) or in the PCB database (when you're running forward–annotation).

If you added component or net attributes to either the schematic or the PCB database, you can also use forward–annotation or back–annotation to add or change these attributes in the target database. You need to know the names of any attributes that were added so you can add them to the *ECO* screen.

You can view, but not change, the names of the *Update* command file, the backup PCB file, and the report file. The names for these files are system–assigned. By default, the name of the *Update* command file is the name of the current design directory with the .upd extension. The name for the backup PCB database is the same name as the original PCB with a .pbk extension. The name for the report is the current design directory name with an .eco extension.

To forward–annotate or back–annotate a database

1. Cycle to Forward Annotation or Back Annotation in the *ECO* screen.

2. Fill the Update Net Names check box to make net names in both databases consistent.

3. Fill the Run Compare check box to have the system run the compare/analyze function and create the update command file.

4. Fill the Run Update check box to have the system update the schematic or PCB database.

5. For back annotation, Fill the Run PC-BACK check box to update the schematic with any swap information from the PCB.

6. Add or delete attributes in the Attributes list box as needed.

To add attributes

Adding component or net attributes is the same for either forward–annotation or back–annotation. By adding attributes, you're telling *ECO* to check whether it needs to add these attributes to parts in the PCB database (for forward–annotation) or the schematic database (for back–annotation).

[1] Cycle to *Component Attributes* or *Net Attributes* next to the Attributes list box.

[2] Select *ADD* next to the Attributes list box.

[3] Enter the attribute name in the data entry box. If you enter all, the system adds attributes in the database. You can also specify a file containing the attributes by entering **@*filename***, where *filename* is the name of the attribute file.

To delete attributes

[1] Select the attribute name in the Attribute list box.

[2] Slect *DELETE.*

7. To run *PC–BACK* with *Back–Annotation*, fill the Run *PC–BACK* check box.

8. Select *RUN.*

When you run *ECO*, it reads the design files, automatically creates and links netlists, packages the schematic, and compares the netlists. It produces a backup PCB file, *filename*.pbk; an *Update* command file, *filename*.upd; and a report file, *filename*.eco; and sends processing and status messages to pcad.log. When you run *Update*, *ECO* also executes the *Update* command file to annotate the database. When you run *PC–BACK*, it insures that all reference designators in the schematic match those in the PCB. Additional sections in this chapter explain more about what happens when you run *ECO, Update*, and *PC–BACK*.

Exiting the *Engineering Change Order* Tool

To exit the *Engineering Change Order* Tool

- Select *EXIT* on the *ECO* screen.

The P–CAD opening screen is then displayed. You can use other P–CAD features to work with the PCB design.

Looking at the Annotation Output

When you're updating a PCB database, *ECO* creates a new layer named $*ECO* that contains symbols indicating changes to the database. If an $*ECO* layer already exists, all current information is erased and only the new information appears.

You can use the PCB Editor in the PCB Tools module to look at the $*ECO* layer.

The $*ECO* layer can contain the following symbols:

- ○ shows pins that had traces connected to them and that *ECO* uncommitted; the pins are uncommitted from the connecting net. (The wire is still there.) Use *Edit* ! *Delete Segment* in the PCB Editor to remove the traces from the pins.
- ✖ appears at the location of pins that had no connecting traces and that *ECO* uncommitted; the pins are uncommitted from the connecting net. No action is required.
- ✚ appears at the location of pins that are added to nets and that need to be wired. Use *Enter* ! *Wire* or *Edit* ! *Enter Wire* to wire the pins to the nets.
- ⊕ shows pins that had traces connected to them and that *ECO* committed; they are now committed to different nets. Remove the traces from the pins and wire the pins to the new nets.
- ✹ shows pins that had no connecting traces and that *ECO* uncommitted; they are now committed to different nets. Wire the pins to the new nets.

- A highlighted box surrounds parts that you should delete.

Power and ground pins aren't marked, and they're not uncommitted automatically.

Figure 7-2 shows the symbols that appear on the $*ECO* layer.

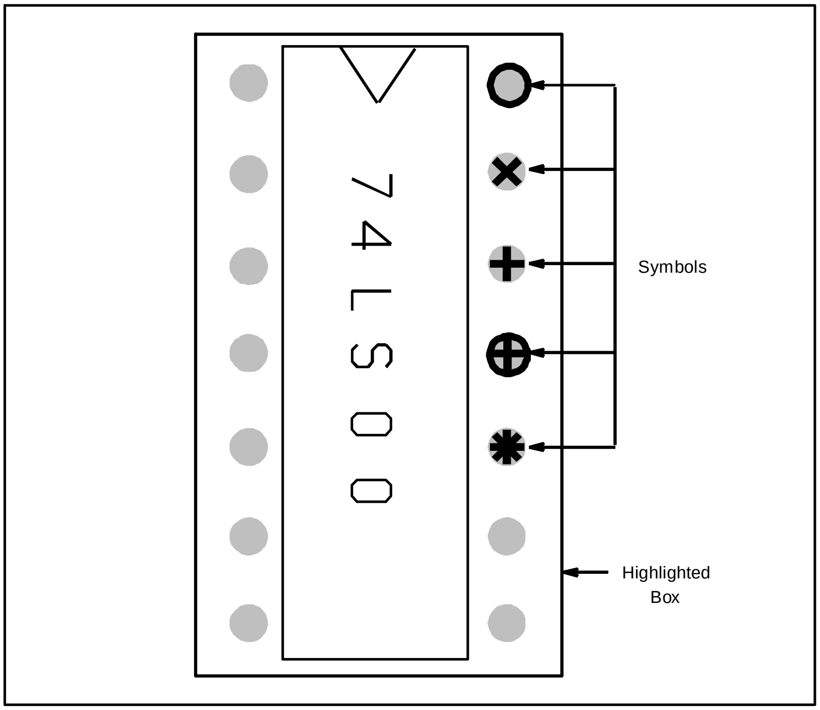

Figure 7-2. Symbols on the $ECO Layer

Understanding the *Update* Command File

When you run *ECO*, the system automatically creates an *Update* command file (*filename*.upd). It contains the commands that *ECO* executes if you choose the option *Run Update.* Executing these commands makes the two databases consistent. For more information, refer to "What Happens When You Run *Update*" in this chapter.

If you don't run *Update* when you run *ECO*, you can check the *Update* command file before you update the schematic or PCB database. Viewing the update file before updating allows you to verify the changes first. You can view the *Update* command file using *Report Editor* in the Design Manager (if you didn't run *Update*). Otherwise, you can view the *Update* commands in the log file (see Reading the *Update* Log File at the end of this chapter).

Figure 7-3 shows a sample *Update* command file. Refer to the descrip– tions in *Update* Commands in this chapter for details on what each command does.

```
LOAD eco1g.pcb
SAVE eco1g.pbk
LOAD eco1g.pcb
DELETE NET /N BBB
DELETE NET /N AAA
DELETE NET /N AAO
DELETE NET /N AA
DELETE NET /R U1 3
DELETE NET /N PIN10
NAME NET NO3 /R U2 2
NAME NET NO /R P1 8
DELETE PIN  U1 2
DELETE PIN  U2 2
DELETE PIN  U1 1
DELETE PIN  U7 11
DELETE PIN  U2 1
HIGHLIGHT PART CN2 ECO1
HIGHLIGHT PART U7 ECO2
HIGHLIGHT PART U1 ECO3
ADD PART 74ls04.prt U4
ADD PART 74ls32.prt U23
ADD PART 74ls08.prt U22
ADD NET /N NO2
            (
            U4 1
            U23 3

ADD NET /N UN000015      >
            (
            UN5 8

ADD NET /N UN000014      >
            (
            UN5 9

ADD NET /N DDO           >
            (
            UN5 4

ADD NET /N DD            >
            (
            UN5 3

ADD PIN UN5 7 GND
ADD PIN UN5 14 +5V
ADD PIN U2 1 NO3
ADD PIN U23 2 NO3
ADD PIN U23 1 NO
ADD PIN U4 2 N1
ADD PIN U2 2 D
ADD PIN U4 14 +5V
ADD PIN U4 7 GND
ADD PIN U23 14 +5V
ADD PIN U23 7 GND
ADD PIN U22 14 +5V
ADD PIN U22 7 GND
SAVE eco1g.pcb
```

Figure 7-3. Sample Update Command File

Following are guidelines to keep in mind while you're viewing the *Update* command file.

- You can add comment lines anywhere in the *Update* command file by entering a percent sign (%). *ECO* ignores all text from the percent sign to the end of the line.

- You can continue a command on the next line in the *Update* command file. Use a right angle bracket (>) at the end of the line to be continued, preceded and followed by a space.
- All commands to be executed must be between a *LOAD* command and a *SAVE* command. Commands that come after a *SAVE* command can cause errors or can cause the *Update* file not to run.
- Pin numbers can have up to seven characters. Filenames can have eight characters plus a three–character extension. Other object identifiers (pin names, net names, gate names, reference designator suffixes, and attribute keywords) can have up to 23 characters if names are assigned using a *Name* command. The system truncates names that are too long and sends a warning message to pcad.log.

Update Commands

This section describes the commands that appear in the *Update* command file used during forward–annotation and back–annotation. The commands appear in alphabetical order.

ADD NET (Forward–Annotation)

ADD NET adds a new named or unnamed net to the PCB database.

Specify the pins in the net by providing the part name and the pin number in pairs. The /U option indicates that the net is unnamed; the /N option means the net has a name. The syntax is

ADD NET /N *netname* (*partname pin# [partname pin#* ...])

For example:

ADD NET /U (U1 1 U2 1 U3 1) (unnamed net)

ADD NET /N NET1 (U1 1 U2 1 U3 1) (named net)

When it’s executing this command, *ECO* checks whether the given net name or part exists in the database, checks whether or not the specified pin with the pin number (for the PCB) is committed to another net, and then adds the pins to the net.

The $*ECO* layer contains a + where pins were added.

ADD PART (Forward–Annotation)

ADD PART adds a part to the PCB database. Specify the part to be added using its filename and the part name you want to assign to the part.

The syntax is

ADD PART *part_filename partname*

For example:

ADD PART 7400.prt U1

When it's executing this command, the program locates the part file, checks whether the part name is already used in the database, and, if not, adds the part to the database.

ADD PIN (Forward–Annotation)

ADD PIN adds a pin to a net in the PCB database. Specify the pin to be added to the net as a part name and pin number pair. You must supply the net name. The syntax is

ADD PIN *partname pin# netname*

For example:

ADD PIN U1 1 NET1

The $*ECO* layer then contains a + at the locations where pins were added to the nets.

ASSIGN ATTR (Forward–Annotation and Back–Annotation)

ASSIGN ATTR assigns attributes to parts in both schematic and PCB databases.

In the schematic database, you can assign an attribute to a single gate using the following options:

- Specifying the gate by its name (assigned using *Enter*!*Name*!*Component* in the Schematic Editor) with the /G option. The syntax is

  ASSIGN ATTR /G gatename keyword=value

For example:

ASSIGN ATTR /G A1 TEST=XXXX

- Specifying the net attribute keywords and values. The syntax is

    ASSIGN ATTR /N <netname> <keyword><valuestring>

For example:

    ASSIGN ATTR /N NET1 WIDTH=12

- Specifying the gate by its reference designator and section assignment pair with the /S option. The syntax is

    ASSIGN ATTR /S refdes sect keyword=value

For example:

    ASSIGN ATTR /S U1 A TEST=XXXX

- Specifying the gate by its location in the database with the /L option. The syntax is

    ASSIGN ATTR /L x y keyword=value

For example:

ASSIGN ATTR /L 300 400 TEST=XXXX

You can assign an attribute to multiple gates with the same reference designator using the /R option. The syntax is

ASSIGN ATTR /R refdes keyword=value

For example:

ASSIGN ATTR /R U1 TEST=XXXX

In the PCB database, you can assign an attribute to a single part using the following options:

- Specifying the part by its name with the /R option. The syntax is

  ASSIGN ATTR /R partname keyword=value

For example:

ASSIGN ATTR /R U1 TEST=XXXX

- Specifying the part by its location in the database with the /L option. The syntax is

  ASSIGN ATTR /L x y keyword=value

For example:

ASSIGN ATTR /L 300 400 TEST=XXXX

A summary of the syntax follows.

In the schematic database, you assign an attribute to a single part as follows:

ASSIGN ATTR /G *gatename keyword=value*
ASSIGN ATTR /S *refdes sect keyword=value*
ASSIGN ATTR /L *x y keyword=value*
ASSIGN ATTR /R *refdes keyword=value*

For the PCB database, you assign an attribute to a single part as follows:

ASSIGN ATTR /L *x y keyword=value*
ASSIGN ATTR /R *partname keyword=value*

where

x and *y* are *X* and *Y* coordinates of the gate or part location.

gatename is the name of the gate.

partname is the name of the part.

refdes is the reference designator.

sect is the section name.

When it's executing this command, the program finds the part or parts and either adds or updates the attribute.

If the attribute already exists, the updated attribute remains on the existing layer and retains the same text attributes (size, justification, rotation, and mirror). If the attribute is new, it's put on the ATTR layer with default text attributes. Refer to the chapter on packaging the schematic in the *Schematic Tools* manual for details.

Critical path information is passed with the attributes in forward–annotation. *ECO* assigns critical path information the reserved keywords $PTHxxx, where xxx is 001, 002, 003, and so on.

Group information is passed with the attributes in forward–annotation. It has the reserved keywords $GRPxxx, where xxx is 001, 002, 003, and so forth.

ASSIGN REFD (Back–Annotation)

ASSIGN REFD either assigns new or updates existing reference designators and pin numbers of a gate in the schematic database.

You can indicate the gate for packaging information by specifying the location of the gate in the schematic database with the /L option or by specifying the gate name with the /G option.

The syntax is as follows:

By location:

ASSIGN REFD /L *x y refdes* (*pin# pname* [*pin# pname*...])

For example:

ASSIGN REFD /L 300 400 U1 (1 INA 2 INB 3 OUTY)

By name:

ASSIGN REFD /G *gname refdes* (*pin# pname* [*pin# pname*...])

For example:

ASSIGN REFD /G A1 U1 (1 INA 2 INB 3 OUTY)

where

x and *y* are *X* and *Y* coordinates of the gate location.

gname is the name of the gate.

refdes is the reference designator.

pin# pname are the physical pin number and the gate pin name. The pin with the pin name (*pname*) is assigned the physical pin number *(pin#)*.

When it's executing this command, *ECO* finds the gate to which the packaging information is assigned, checks whether the number of pins is valid, checks whether the gate has a pin with the given pin name, and adds?the packaging information to the gate. If the gate has any existing packaging information, *ECO* deletes the existing packaging information before adding the new information.

DELETE NET (Forward–Annotation)

DELETE NET deletes a net from the PCB database. You can specify the net to be deleted from the PCB database as follows:

- With the name of the net and the /N option. The syntax is

    DELETE NET /N *netname*

For example:

    DELETE NET /N GND

- With the part name, pin number, and /R option. The net deleted is then the net to which the pin is committed. The syntax is

    DELETE NET /R *partname pin#*

For example:

    DELETE NET /R U1 1

When it's executing this command, the program locates the specified net, uncommits the pins from the net, and deletes the net from the database.

DELETE PART (Forward–Annotation)

DELETE PART deletes a part in the PCB database. The syntax is

DELETE PART *part_name*

For example:

DELETE PART U1

When it's executing this command, the program locates the part in the database, uncommits any committed pins of the part, and deletes the part.

ECO doesn't delete parts during forward–annotation. Instead, it issues a *HIGHLIGHT PART* command that highlights parts with a box on the $*ECO* layer. You can delete the parts by

- Replacing the *HIGHLIGHT PART* command in the *Update* command file with the *DELETE PART* command.
- Manually inserting the *DELETE PART* command in the *Update* command file.

- Using the PCB Editor.

The $*ECO* layer contains a highlighted box at the locations of parts that were deleted:

DELETE PIN (Forward–Annotation)

DELETE PIN uncommits a pin from a net in the PCB database. The syntax is

DELETE PIN *partname pin#*

For example:

DELETE PIN U1 1

When it's executing this command, the program checks whether the reference designator and pin number are valid, and if the pin is committed, uncommits the pin from the net. After deleting the pin from the net, if the net has no more pins, *ECO* processes the net as a *DELETE NET* command.

The $*ECO* layer contains a circle or X at the locations of pins that were uncommitted from connecting nets.

HIGHLIGHT PART (Forward–Annotation)

HIGHLIGHT PART highlights a part on the $*ECO* layer of the PCB database by drawing a box on the outline of the part. A highlighted part in forward–annotation indicates that the part doesn't participate in logic and can be deleted from the PCB.

You specify the part to be highlighted using the reference designator.

The syntax is

HIGHLIGHT PART *old_refdes new_refdes*

where

old_refdes is the reference designator that is then highlighted.

new_refdes is the new reference designator to be given to the part being highlighted. You supply a new name for the part to avoid name conflicts that could occur as a result of other *Update* commands.

For example:

HIGHLIGHT PART U1 *ECO*1

When it's executing this command, *ECO* checks that no part in the database has the *new_refdes*, finds the part in the database with the *old_refdes*, highlights the part, and renames the part with the new name.

LOAD (Forward–Annotation and Back–Annotation)

LOAD loads a schematic or PCB database. The syntax is

LOAD *filename*

where *filename* is a database filename including the path.

For example:

LOAD test.pcb

When it's executing this command, the program checks whether the file is a valid P–CAD database, saves the previously opened database, if any, and loads the specified database.

NAME NET (Forward–Annotation and Back–Annotation)

NAME NET names or renames nets in both schematic and PCB databases. The pin of a net is used to identify the net to be named or renamed.

In the schematic database:

- You identify the pin of a gate by giving the gate name and pin number. The syntax is

  NAME NET *netname* /G *gatename pin#*

For example:

NAME NET GND /G G1 1

- You identify the pin of a gate by giving the reference designator and packaged pin number. The syntax is

  NAME NET *netname* /R *refdes pkgpin#*

For example:

NAME NET GND /R U1 1

In the PCB database:

You identify the pin of the part by giving the part name and the pin number. The syntax is

NAME NET *netname* /R *partname pin#*

For example:

NAME NET GND /R U1 1

When it's executing this command, the program checks to make sure that the reference designator (part name) and pin number are valid for the /R option, and that the component name and pin number are valid. The program also checks that no other net in the database has the given net name, and then assigns the name to the net.

SAVE (Forward–Annotation and Back–Annotation)

SAVE saves a schematic or PCB database. The syntax is

SAVE *filename*

where *filename* is a database filename including the path.

For example:

SAVE test.pcb

When it's executing this command, the program checks the validity of the filename given, and saves the current database that was loaded.

SWAP NET (Forward–Annotation and Back–Annotation)

SWAP NET swaps the names of two nets. The syntax is

SWAP NET *netname1 netname1*

For example:

SWAP NET NET1 NET2

When it's executing this command, the program checks to make sure that nets with the given names exist and swaps the net names of the two nets.

SYSTEM (Forward–Annotation and Back–Annotation)

SYSTEM is implemented in both forward– and back–annotation, but affects the critical path information only in PCB databases. The syntax is

SYSTEM *system_name*

For example:

SYSTEM PCAD
SYSTEM NONPCAD

ECO automatically sends this command to the update file with the *system_name* as PCAD. This command is the first one in the update file, and it should occur only once. The command doesn't affect back– annotation; schematic databases (*filename*.sch) aren't affected.

In forward–annotation, if *system_name* is P–CAD, each time a PCB database is loaded for updating, the critical path information is deleted and the PCB database is updated with the critical path information specified in the update file. If *system_name* is NONPCAD, the critical path information in the update file is added and updated. Previous critical path information in the PCB isn't deleted.

Running *PC–BACK* from the Command Line

Command line mode allows you to specify the input swap report file (*filename*.rpt), PC–BACK instruction file (*filename*.bck), and the output back–annotation file (*filename*.bka), when you run *PC–BACK*. To use command line mode, return to the main Design Manager screen and select the *DOS Shell* button. Be sure you are in the same directory as the files you are working on.

At the DOS prompt type **pcback** followed by the three filenames and press ↵. For example:

pcback test1.rpt test1.bck test1.bka

After you enter the command line, *PC–BACK* runs automatically with no forther input from you. It displays progress and error messages, if any. When processing is complete, the system returns to DOS.

Creating a Batch File

A batch file can contain the command line instructions for running the program several times consecutively. Use a text editor to create the ASCII batch file. Each line in the file is the same format used for a command line.

You must use a .bat as the filename extension when naming the batch file. Figure 7-4 shows a sample batch file named back.bat which is in the \pcad\proj0 directory.

```
pcback test1.rpt test1.bck test1,bka
pcback test2.rpt test2.bck test1.bka
pcback test3.rpt test2.bck test1.bka
```

Figure 7-4. Sample Batch File

To run the batch file, at the DOS prompt type the filename and press ↵. For example, to run the example, back.bat, from any directory you would type

\pcad\proj0\back ↵

The program runs as many times as the number of command lines listed in the batch file. When processing is complete, the system returns to DOS.

Interpreting the *ECO* Report File

This section describes each section of the *ECO* report file (*filename*.eco). The *ECO* report file includes the Compare/Analyze report and the *Update* log file. First a complete sample report is shown, then sections of the report are described.

ECO always appends to the end of the report file so that you can maintain a history of all runs. Because this file can get very large, you need to delete it occasionally or archive it to save disk space. Figure 7-5 shows a sample output file.

```
%*****************************************************************************************
%                                                                    *
% Program            :  PC*CPR VERSION 8.0  COMPARE/ANALYZE                        *
% Date               :  Aug 15 1994                                   *
% Time               :  10:56:44                                    *
% Schematic Netlist   :  eco1g.bnl                                       *
% PCB Netlist         :  eco1g.pnl                                      *
% Part Reference File  :  eco1.fil                                       *
% Comparison Mode      :  Forward Annotation                                  *
%                                                                    *
%*****************************************************************************************
cpr Report
----------
Schematic Netlist                        PCB
-----------------    -----------
eco1g.bnl                  eco1g.pnl
Number of Gates            21            Number of Parts
Number of Nets             15            Number of Nets
Number of Suspect Gates    2             Number of Suspect Gates     4
Number of Suspect Nets     9             Number of Suspect Nets      10
Number of Spare Gates      1             Number of Spare Gates       15
Number of Floating Nets    0             Number of Floating Nets     0
==========================================================================================
GATE REPORT
==========================================================================================
*** SYSTEM NAMED PARTS ON PCB **********************************************************
*****************************************************************************************
*
*  THE FOLLOWING PARTS IN THE PCB DATABASE MUST BE NAMED BY THE USER              *
*
*****************************************************************************************
Part Type      Ref Des
---------      -------
bfcap.prt      UC000004
ckO5A.prt      UC000003
ck05A.prt      UC000002
bfcap.prt      UC000001
bfcap.prt      UC000000
*** GATES ON SCHEMATIC NOT ON PCB ********************************************************
Reference Designator:  U4
--------------------

                 Gate         Schematic     Logical      Pin
Symbol Type      Name         Sheet         Pin Name     Number    Net Name
------------     ---------    ----------    ---------    -------   ---------

74ls04.sym       UC000022     eco1g.sch     IN           1         NO2
                                            OUT          2         N1
```

Figure 7-5. Sample ECO Report Output File

```
Reference Designator:  U23
---------------------

                   Gate           Schematic      Logical        Pin
Symbol Type        Name           Sheet          Pin Name       Number      Net Name
------------       ---------      ----------     ---------      -------     ---------

74LS32.sym         $0000001       eco1g.sch      INA            1           NO
                                                 INB            2           NO3
                                                 OUTY           3           NO2

*** GATES ON PCB NOT ON SCHEMATIC ****************************************************
Reference Designator:  UN5
--------------------
Part Type    Ref Des  Pin Number  Net Name
-----------  -------- ----------  --------
74ls04.prt   UN5           1          AAA
                2          BBB
Reference Designator:  U7
--------------------
Part Type    Ref Des   Pin Number  Net Name
-----------  --------  ----------  --------
74ls04.prt   U7            11         N1
                10         PIN10
Reference Designator:  CN2
--------------------
Part Type    Ref Des   Pin Number  Net Name
-----------  --------  ---------- --------
CE100.prt    CN2           1          AA
                           2
Reference Designator:  U1
--------------------
Part Type    Ref Des  Pin Number  Net Name
-----------  -------- ----------  --------
74ls32.prt   U1            1          B
                2          C
                3          UN000013
*** SPARE GATES ON SCHEMATIC ****************************************************************

                   Schematic        Gate
Symbol Type        Sheet            Name          Ref Des      Pin Numbers
------------       ----------       ---------     --------     ------------

74LS08.sym         eco1g.sch        UC000026      U22          ( 1  2  3 )

*** SPARE GATES ON PCB **********************************************************************
Part Type    Ref Des  Pin Numbers
-----------  -------- ----------
74ls00.prt   U2     ( 9     10     8 )
74ls00.prt   U2     ( 12     13     11 )
74ls32.prt   U1     ( 4     5     6 )
74ls32.prt   U1     ( 9     10     8 )
74ls32.prt   U1     ( 12     13     11 )
74ls08.prt   U3     ( 9     10     8 )
74ls08.prt   U3     ( 12     13     11 )
74ls04.prt   U7     ( 1     2 )
74ls04.prt   U7     ( 3     4 )
74ls04.prt   U7     ( 5     6 )
74ls04.prt   U7     ( 9     8 )
```

Figure 7-5. Sample ECO Report Output File (cont'd)

```
74ls04.prt   U7     ( 13     12 )
74ls04.prt   UN5     ( 5      6 )
74ls04.prt   UN5     ( 11     10 )
74ls04.prt   UN5     ( 13     12 )



==========================================================================================
NET REPORT
==========================================================================================
*** NETS FOUND ONLY ON SCHEMATIC *********************************************************
NO2   UN000015   UN000014      DDO       DD
NO3       NO
*** NETS FOUND ONLY ON PCB ***************************************************************
  BBB     AAA      AAO      AA   UN000013
PIN10       C        B
*** NETS FOUND IN BOTH NETLISTS BUT NOT THE SAME *****************************************
Net Name:  N1
---------
Pins found on Schematic but not on PCB




Logical                                  Gate            Schematic
Pin Name       Symbol Type               Name            Sheet           Ref Des       Pin Number
---------      ------------              --------        ---------       --------      -----------

IN             74ls04.sym                UC000022        eco1g.sch       U4            2

 Pins found on PCB but not on Schematic
 Logical
 Pin Name  Part Type    Ref Des   Pin Number
 --------  -----------  --------  ----------
 IN       74ls04.prt    U7       11
 Net Name:  D
 ---------
 Pins found on Schematic but not on PCB



 Logical                                  Gate            Schematic
 Pin Name       Symbol Type               Name            Sheet           Ref Des       Pin Number
---------      ------------              --------        ---------       --------      -----------

 INA            74ls04.sym                $0000010        eco1g.sch       U2            2


 Pins found on PCB but not on Schematic
 Logical
 Pin Name  Part Type    Ref Des   Pin Number
 --------  -----------  --------  ----------
 INA      74ls00.prt   U2        1
 *** NETS FROM PWGD ATTRIBUTE OR PIN=NET OPTION
 **********************************************
 The following suspect nets were assigned to components and pins by
 the PWGD attribute or the PIN=NET option in the cross reference file.
 All the component types that have PIN=NET with net: +5V
 All the component types that have PIN=NET with net: GND
```

Figure 7-5. Sample ECO Report Output File (cont'd)

```
**********************************************************************
*                                             *
*                                             *
*    Program  :   PC*UPD VERSION 8.0                    *
*    Date     :   Aug 15 1994                   *
*    Time     :   10:56:48 AM                   *
*    File In  :   eco1g.upd                   *
*    File Out :   eco1g.eco                   *
*    Format   :   upd LOG FILE                   *
*                                             *
**********************************************************************
001: LOAD eco1g.pcb
002: SAVE eco1g.pbk
003: LOAD eco1g.pcb
004: DELETE NET /N BBB
005: DELETE NET /N AAA
006: DELETE NET /N AAO
007: DELETE NET /N AA
008: DELETE NET /R U1 3
009: DELETE NET /N PIN10
010: NAME NET NO3 /R U2 2
011: NAME NET NO /R P1 8
012: DELETE PIN  U1 2
013: DELETE PIN  U2 2
014: DELETE PIN  U1 1
015: DELETE PIN  U7 11
016: DELETE PIN  U2 1
017: HIGHLIGHT PART CN2 ECO1
018: HIGHLIGHT PART U7 ECO2
019: HIGHLIGHT PART U1 ECO3
020: ADD PART 74ls04.prt U4
021: ADD PART 74ls32.prt U23
022: ADD PART 74ls08.prt U22
023: ADD NET /N NO2                    >
024:    (                              >
025:     U4 1                          >
026:     U23 3                         >
027:    )
028: ADD NET /N UN000015               >
029:    (                              >
030:     UN5 8              >
031:    )
032: ADD NET /N UN000014               >
033:    (                              >
034:     UN5 9                         >
035:    )
036: ADD NET /N DDO         >
037:    (                   >
038:     UN5 4                         >
039:    )
040: ADD NET /N DD                     >
041:    (                              >
042:     UN5 3              >
043:    )
044: ADD PIN UN5 7 GND
045: ADD PIN UN5 14 +5V
046: ADD PIN U2 1 NO3
047: ADD PIN U23 2 NO3
048: ADD PIN U23 1 NO
049: ADD PIN U4 2 N1
050: ADD PIN U2 2 D
051: ADD PIN U4 14 +5V
052: ADD PIN U4 7 GND
053: ADD PIN U23 14 +5V
054: ADD PIN U23 7 GND
055: ADD PIN U22 14 +5V
056: ADD PIN U22 7 GND
057: SAVE eco1g.pcb
Warning - Pin at 850 1050 was connected to a wire.
Warning - Pin at 2050 1050 was connected to a wire.
Warning - Pin at 850 1150 was connected to a wire.
Warning - Pin at 2050 1150 was connected to a wire.
```

Figure 7-5. Sample ECO Report Output File

Using the Compare/Analyze Report (CPR)

The Compare/Analyze (CPR) portion of the *ECO* report lists the results of the comparison and analysis process, and the differences between the schematic and PCB netlists.

During forward–annotation, *ECO* creates an *Update* command file to update the PCB database. After *ECO* runs the command file, the differences are automatically corrected. Therefore, if you run *Update* as part of the forward–annotation process, you don't have to refer to the CPR report.

During back–annotation, however, *ECO* doesn't automatically correct the differences reported in the schematic database. Use the CPR report in this case to find out what manual changes you need to make to the schematic.

Use the sections in the report as checklists. Check each item listed in the report, locate it in the schematic and PCB databases, and make the necessary changes until the two databases are in step. Refer to the *PCB Tools* and *Schematic Tools* manuals for information about making the changes.

After initially running forward–annotation or back–annotation, viewing the report, and fixing any discrepancies, rerun *ECO* to make sure the changes you made are correct. The new report should no longer show any discrepancies between the two databases.

The CPR report contains the following information:

- a summary of the number of gates and nets in the schematic and PCB databases
- all the unmatched gates and nets that are reported as logic changes
- spare gates from both the schematic and PCB databases
- floating nets from both the schematic and PCB databases

The Gate report contains these sections:

- *System–Named Parts On PCB*
- *Gates on Schematic Not on PCB*
- *Gates on PCB Not on Schematic*
- *Gates in Both Netlists but Not Matching*
- *Spare Gates on Schematic*
- *Spare Gates on PCB*
- *Parts with COMPARE=MECH Attribute*
- *Gates and Parts with Missing Packaging Information*
- *Inconsistent Pin LEQ Values in Back–Annotation*

The Net report contains these sections:

- *Nets Found Only on Schematic*
- *Nets Found Only on PCB*
- *Floating Nets on Schematic*
- *Floating Nets on PCB*
- *Nets Found in Both Netlists but Not the Same*
- *Nets from PWGD Attribute on PIN=NET Option*

Compare/Analyze Report

Figure 7-6 shows a sample CPR report. In the report,

- *Number of Gates* is the total number of gates in the schematic netlist.
- *Number of Parts* is the total number of parts in the PCB netlist.
- *Number of Nets* is the total number of nets in each netlist.
- *Number of Suspect Gates* is the number of gates that don't match gates in the other netlist.
- *Number of Suspect Nets* is the number of nets that don't match nets in the other netlist.
- *Number of Spare Gates* is the number of gates that aren't connected to any net in each netlist.
- *Number of Floating Nets* is the number of nets that aren't connected to any gate in each netlist.

```
%******************************************************************************
%                                                                            *
% Program            :  PC*CPR VERSION 8.0                                   *
% Date               :  Aug 15 1994                                          *
% Time               :  12:17:32                                             *
% Schematic Netlist  :  temp.bnl                                             *
% PCB Netlist        :  6020101.pnl                                          *
% Part Reference File :  6020.fil                                            *
% Comparison Mode    :  Back Annotation                                      *
%                                                                            *
%******************************************************************************

cpr Report
 ----------
Schematic Netlist            PCB Netlist
-----------------     -----------
temp.bnl                     6020101.pnl
Number of Gates                            76            Number of Parts
Number of Nets                             70            Number of Nets
Number of Suspect Gates      0             Number of Suspect Gates     4
Number of Suspect Nets       10            Number of Suspect Nets      10
Number of Spare Gates        0             Number of Spare Gates       21
Number of Floating Nets      1             Number of Floating Nets     2
```

Figure 7-6. Sample CPR Report

Gate Report

Figure 7-7 shows the section of the Gate report that lists all the components with no packaging information, all the gate and part types with inconsistent pin LEQs, and all the system–named parts in the PCB netlist.

```
        ================================================================
                                GATE REPORT
        ================================================================
*** SCH GATES WITH NO PACKAGING INFORMATION**********************
      74ls08.sym
*** PCB PARTS WITH NO PACKAGING INFORMATION***********************
      74ls00.prt
*** SCH GATES AND PCB PARTS WITH INCONSISTENT PIN LEQ VALU*********
Symbol Type      Part Type
-----------      ---------
74ls00.sym       74ls00.prt
74ls21.sym       74ls31.prt
- - - - -        74ls04.prt
  inv.sym        74ls31.prt
  nand.          74ls31.prt
*** SYSTEM NAMED PARTS ON PCB ************************************
******************************************************************
*
*  THE FOLLOWING PARTS IN THE PCB DATABASE MUST BE              *
*   NAMED BY THE USER
*
******************************************************************
Part Type   Ref Des
---------   -------
bfcap.prt   UC000004
cko5a.prt   UC000003
cko5a.prt   UC000002
bfcap.prt   UC000001
bfcap.prt   UC000000
```

Figure 7-7. System-named Parts on PCB

In the report,

- *Symbol Type* is the symbol filename of the gate.
- *Part Type* is the part filename.
- *Reference Designator* is the system–assigned part name.

Figure 7-8 shows the section of the Gate report that lists all the gates that are in the schematic netlist but aren’t in the PCB netlist.

- *Reference Designator* is the name you assign to the gate using *Enter*!*Ref. Des. & Section*.
- *Symbol Type* is the symbol filename of the gate.
- *Gate Name* is either the gate name you assign using *Name*!*Component* in the Schematic Editor, or a system–assigned name.
- *Schematic Sheet* is the name of the schematic sheet or third–party macro that the gate is in.
- *Logical Pin Name* is the logical pin name you assign to a pin using *Enter*!*Pin* in the Symbol Editor.
- *Pin Number* is the physical pin number you assign to the pins using *Enter*!*Packaging Data*.

- *Net Name* is either the name of the net connected to the gate you assign using *Name* ! *Net* in the Schematic Editor, or a system–assigned name.

```
*** GATES ON SCHEMATIC NOT ON PCB ************************
Reference Designator:  U1
---------------------



                  Gate         Schematic    Logical     Pin
Symbol Type       Name         Sheet        Pin Name    Number    Net Name
-----------       ---------    ---------    ---------   ------    ---------
7404.sym          UC000007     e1.sch       INA         9         Y1
                                            OUTY        8         Y2
```

Figure 7-8. Gates on Schematic Not on PCB

Figure 7-9 shows the section of the gate report that lists all the gates in the PCB netlist but not in the schematic netlist. The parts are listed in gate format.

- *Reference Designator* is either the part name you assign using *Enter* ! *Ref. Des. & Section* in the Schematic Editor or a system–assigned name.
- *Part Type* is the part definition of the part.
- *Pin Number* is the physical pin number.
- *Net Name* is either the name of the net connected to the part you assign using *Enter* ! *Name* ! *Net* in the Schematic Editor, or a system– assigned name.

```
*** GATES ON PCB NOT ON SCHEMATIC ************************
Reference Designator:  U2
---------------------



           Part Type     Ref Des      Pin Number     Net Name
           ----------    --------     ----------     ---------
           7404.prt      U2           13             nothing
                                      12             Z1
```

Figure 7-9. Gates on PCB Not on Schematic

Figure 7-10 shows the section of the Gate report that lists all the gates that are in both the schematic and the PCB netlists but that aren’t the same.

- *Reference Designator* is either the name you assign to the gates using *Enter* ! *Ref. Des. & Section*, or a system–assigned name.

- *Symbol Type* is the symbol filename of the gate.
- *Part Type* is the part filename.
- *Gate Name* is either the gate name you assign using *Name*! *Component* in the Schematic Editor, or a system–assigned name.
- *Schematic Sheet* is the name of the sheet or macro that the gate is in.
- *Logical Pin Name* is the logical pin name you assign using *Enter*! *Pin* in the Symbolic Editor.
- *Pin Number* is the physical pin number you assign using *Enter*! *Packaging Data*.
- *Net Name* is either the name of the net connected to the gate you assign using *Name*! *Net* in the Schematic Editor, or a system–assigned name.

```
*** GATES IN BOTH NETLISTS BUT NOT MATCHING ***************
Reference Designator:  U4
 --------------------
Gate From Schematic:

                      Gate          Schematic    Logical     Pin
    Symbol Type       Name          Sheet        Pin Name    Number   Net Name
    ------------      ---------     ----------   --------    ------   ---------
    7404.sym          UC000007      e1.sch       INA         9        NET1
                                                 OUTY        8        NET2

Gate From PCB:

                                Logical
    Part Type      Ref Des      Pin Name      Pin Number      Net Name
    ----------     --------     ---------     ----------      ---------
    7404.prt       U4           INA           9               NET1
                                OUTY          8               NET
```

Figure 7-10. Gates in Both Netlists But Not Matching

Figure 7-11 shows the section of the Gate report that lists all the spare gates in the schematic netlist.

```
*** SPARE GATES ON SCHEMATIC ****************************

                       Schematic       Gate
       Symbol Type     Sheet           Name           Ref Des        Pin Numbers
       -----------     ----------      ---------      -------        ------------
       7404.sym        e1.sch          UC000006       U2             ( 11   10 )
```

Figure 7-11. Spare Gates on Schematic

- *Symbol Type* is the symbol filename of the gate.
- *Schematic Sheet* is the name of the schematic sheet or third–party macro in which the gate is located.
- *Gate Name* is either the gate name you assign using *Name*!*Component* in the Schematic Editor, or a system–assigned name.
- *Reference Designator* is the name you assign to the gates using *Enter*!*Ref. Des. & Section.*
- *Pin Number* is the physical pin number you assign using *Enter*!*Packaging Data*.

Figure 7-12 shows the section of the Gate report that lists all the spare gates within parts in the PCB netlist.

- *Part Type* is the part filename.
- *Reference Designator* is either the part name you assign using *Enter*!*Ref. Des. & Section* in the Schematic Editor, or a system–assigned name.
- *Pin Number* is the physical pin number.

```
*** SPARE GATES ON PCB ***********************************
Part Type   Ref Des  Pin Numbers
---------  --------  -----------
34p3m.prt  P3       ( 12 )
34p3m.prt  P3       ( 30 )
34p3m.prt  P3       ( 32 )
```

Figure 7-12. Spare Gates on PCB

Figure 7-13 shows the section of the gate report that lists all the parts with the attribute of COMPARE=MECH in the PCB netlist. Parts that were specified as jumpers are also listed in this section.

- *Part Type* is the part filename.
- *Reference Designator* is either the part name you assign using *Enter*!*Ref. Des. & Section* in the Schematic Editor, or a system–assigned name.

```
*** PARTS WITH COMPARE=MECH ATTRIBUTE *********************
Part Type     Ref Des
---------     --------
34p3m.prt     P6
```

Figure 7-13. Parts With COMPARE=MECH Attribute

Net Report

Figure 7-14 shows the section of the net report that lists all the nets in the schematic netlist but not in the PCB netlist.

- *Net Name* is either the net name you assign using *Name*!*Net* in the Schematic Editor, or a system–assigned name.

```
==========================================================
NET REPORT
==========================================================
*** NETS FOUND ONLY ON SCHEMATIC *************************
      Y1        N4
```

Figure 7-14. Nets Found Only on Schematic

Figure 7-15 shows the section of the net report that lists all the nets in the PCB netlist but not in the schematic netlist.

- *Net Name* is either the net name you assign using *Name*!*Net* in the Schematic Editor, or a system–assigned name.

```
*** NETS FOUND ONLY ON PCB ********************************
       N2
```

Figure 7-15. Nets Found Only on PCB

Figure 7-16 shows the section of the net report that lists all the nets with no connecting pins in the schematic netlist.

- *Net Name* is either the net name you assign using *Name*!*Net* in the Schematic Editor, or a system–assigned name.

```
*** FLOATING NETS ON SCHEMATIC ***************************
    DDD
```

Figure 7-16. Floating Nets on Schematic

Figure 7-17 shows the section of the net report that lists all the nets with no connecting pins in the PCB netlist.

- *Net Name* is either the net name you assign using *Name*!*Net* in the Schematic Editor, or a system–assigned name.

```
*** FLOATING NETS ON PCB ***********************************
     EEE    UN000000
```

Figure 7-17. Floating Nets on PCB

Figure 7-18 shows the section of the net report that lists all the nets in the schematic and PCB netlists that aren't the same.

- *Net Name* is either the net name you assign using *Name*!*Net* in the Schematic Editor, or a system–assigned name.
- *Logical Pin Name* is the logical pin name you assign using *Enter*!*Pin* in the Symbol Editor.
- *Symbol Type* is the symbol filename of the gate.
- *Part Type* is the part filename.
- *Gate Name* is either the gate name you assign using *Name*!*Component* in the Schematic Editor, or a system–assigned name.
- *Schematic Sheet* is the name of the schematic sheet or third–party macro that the gate is in.
- *Reference Designator* is either the gate name you assign using *Enter*!*Ref. Des. & Section,* or a system–assigned name.
- *Pin Number* is the physical pin number you assign using *Enter*!*Packaging Data*.

```
*** NETS FOUND IN BOTH NETLISTS BUT NOT THE SAME **********
Net Name:  N6
---------
Pins found on Schematic but not on PCB


     Logical                      Gate   Schematic
     Pin Name   Symbol Type       Name   Sheet       Ref Des    Pin Number
     ---------  ------------      -----  ---------   --------   ----------
     OUTY       7404.sym          G3     e1.sch      U1         5

Pins found on PCB but not on Schematic
Logical
Pin Name  Part Type   Ref Des   Pin Number
--------  ---------   -------   ----------
 INA      7404.prt    U2        5
```

Figure 7-18. Nets Found in Both Netlists But Not the Same

Figure 7-19 shows the section of the net report that lists all the nets that are suspect in the schematic and PCB netlists. These nets have pins connected to them through the PWGD attribute or the pin–to–net mapping option in the cross–reference file.

- *Net Name* is either the net name you assign using *Name* ! *Net* in the Schematic Editor, or a system–assigned name.

```
*** NETS FROM PWGD ATTRIBUTE OR PIN=NET OPTION ************
The following suspect nets were assigned to components and pins by the
PWGD attribute or the PIN=NET option in the cross reference file.
All the component types that have PIN=NET with net: +5V All the component
types that have PIN=NET with net: GND
```

Figure 7-19. Nets From PWGD Attribute or PIN=NET Option

Reading the *Update* Log File

Update reads the *Update* command file created by *ECO* and updates either the schematic or the PCB database. *Update* echoes each command it executes to the log file in the *ECO* report. The log file is appended to the *ECO* report file (*filename*.eco) when you run *Update*.

The *Update* log file is essentially identical to the *Update* command file, except that a file header is included, each command line is numbered, and error or warning messages are included. You can use the *Update* log file to determine what actions were executed during the update process, and check whether any warning or error messages were issued.

A section of the *Update* log file is shown in Figure 7-20. Refer to Understanding the *Update* Command File and *Update* Commands in this chapter for more information on the *Update* log file.

```
************************************************************
*                                                    *
* Program  :  PC*UPD VERSION 8.0                               *
*          :  Aug 15 1994                          *
* Time     :  09:57:48 AM                          *
* File In  :  eco1g.upd                            *
* File Out :  eco1g.log                            *
* Format   :  upd LOG FILE                           *
*                                                    *
************************************************************
001: LOAD eco1g.pcb
002: SAVE eco1g.pbk
003: LOAD eco1g.pcb
004: DELETE NET /N BBB
005: DELETE NET /N AAA
006: DELETE NET /N AAO
007: DELETE NET /N AA
008: DELETE NET /R U1 3
009: DELETE NET /N PIN10
010: NAME NET NO3 /R U2 2
011: NAME NET NO /R P1 8
012: DELETE PIN  U1 2
013: DELETE PIN  U2 2
014: DELETE PIN  U1 1
015: DELETE PIN  U7 11
016: DELETE PIN  U2 1
017: HIGHLIGHT PART U1 ECO3
018: HIGHLIGHT PART U7 ECO2
019: HIGHLIGHT PART CN2 ECO1
020: ADD PART 74ls04.prt U4
```

Figure 7-20. Update Log File

Update issues warning messages whenever it performs an operation, even though you don't need to do anything. For example, the following message informs you that a pin with a trace routed to it was deleted.

Warning — Pin at 850 1050 was connected to a wire.

This pin is also marked with a circle (at 850 1050) on the $*ECO* layer.

Error messages are issued either because of syntax errors encountered in the *Update* command file or because a certain operation couldn't be performed. For example, the following message indicates that an attempt was made to add a part to a database using a reference designator that was already assigned to an existing part:

```
012: ADD PART 74ls04.prt U3
    Error — Part name U3 already used.
```

The following error message indicates that a command (ADD PART) in the *Update* command file was misspelled:

```
013: AD PART 74ls04.prt U3
    Error — Invalid command keyword.
```

If an error occurs, first verify that the command syntax is correct, then check whether the command was correct for the database it was operating on, and, finally, inspect the database to ensure that a problem isn't in the database. Generally, errors don't occur in *Update* command files created by *ECO*.

Editing Report Files 8

The *Report Editor* button is located at the bottom of the main P–CAD screen so you can easily access it from each module. The Report Editor lets you edit, add, delete, rename, copy, and print report files or other ASCII files. You can use this tool throughout the PCB design process to access and maintain ASCII files associated with each of your PCB designs.

This chapter presents information on the following topics:

- opening the Report Editor screen
- adding a file
- editing or viewing a file
- deleting a file
- renaming a file
- copying a file
- printing a file

The files you work with in the *Report Editor* fall into these categories:

- ASCII files you create, such as a cross–reference files
- ASCII report files generated by the system, such as the Drill Data report
- other system–generated ASCII files, such as pcform.log

Some P–CAD tools require ASCII input files that provide specific design information. You can create ASCII files with the text editor provided here or any other text editor. Some tools have screens that prompt for information stored in ASCII format.

Report files are text files that provide summaries of design reference information, such as a materials list. You can generate reports in various ways in the P–CAD system.

An example of a system–generated file is a PDIF file. This type of file is generated by the Write PDIF File tool. PDIF stands for P–CAD Database Interchange Format.

Opening the Report Editor Screen

You open the Report Editor screen from the main P–CAD screen.

To open the Report Editor screen

- Select *Report Editor.* The Report Editor screen shown in Figure 8-1 is displayed.

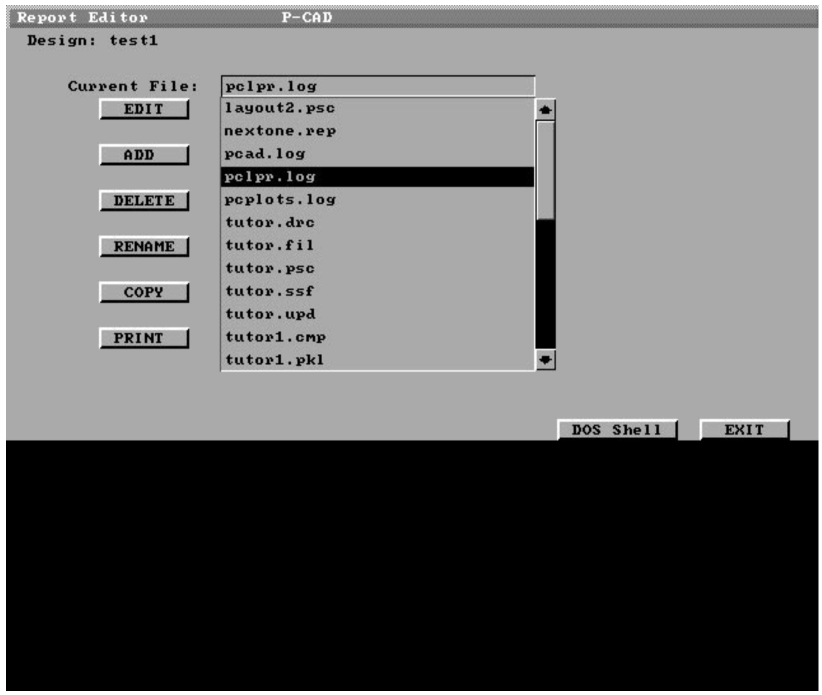

Figure 8-1. Report Editor Screen

The *Report Editor* uses edlin, or any other text editor available on your system. You specify which text editor you want to use in the *System Configuration* tool of the Design Manager module. This section presents some basic information about using the options in the *Report Editor.* For more information about using the editor, refer to the documentation for your text editor.

Adding a File

In order to view or edit a file in the *Report Editor* tool, it must be shown in the list box.

Many of the files you want to access are automatically included in the list box on the Report Editor screen. Some files don't appear in the list box automatically (for example, configuration files). You can add, view, and edit any files by selecting one of the buttons next to the list box.

To create a new file

1. Select *ADD.*
2. Enter the filename and extension of the file you want to use in the Current File data entry box.
3. To display the file for editing, highlight the filename in the list box and select *EDIT.* A text editor screen appears.
4. Edit and save the file within the text editor.
5. Exit the text editor to return to the Report Editor screen.
6. Select *EXIT* to leave the *Report Editor* tool.

To add a system–generated file

1. Select *ADD.*
2. Enter the filename and extension of the file you want to use in the Current File data entry box.

The file is added to the list box alphabetically.

Editing or Viewing a File

The *Report Editor* is particularly useful for reviewing system–generated reports, such as ASCII netlist reports, design rules check (DRC) reports, electrical rules check (ERC) reports, or engineering change order (ECO) reports.

To edit a file

1. Highlight the file you want to edit in the list box.
2. Select *EDIT.* A text editor screen appears.
3. Edit, save, and close the file from within the text editor.
4. Select *EXIT* to leave the *Report Editor* tool.

To view a file

1. Select the file you want to view from the list box.
2. Select *EDIT.* A text editor screen appears.
3. View and then close the file from within the text editor.
4. Select *EXIT* to leave the *Report Editor* tool.

To list files with a specific extension or filename pattern

1. Select the Current File data entry box.
2. Enter the search pattern as *.*ext* where *ext* is the extension; for example, *.pdf. Only those files with the specified extension from the current design directory are shown in the list box.

Deleting a File

You can permanently erase any files that are shown in the list box.

Note: If you want to keep a backup copy of a file, do so before you delete the file.

To delete a file

1. Select the file you want to delete from the list box.
2. Select *DELETE.* The system displays a decision box and prompts you to confirm your action.
3. Select *YES* if you want to delete the file from the disk.
4. Select *NO* to cancel the action.

Renaming a File

You can rename any files displayed in the list box.

To rename a file

1. Highlight the file you want to rename in the list box.
2. Select *RENAME.*
3. Enter the new filename and extension in the Current File data entry box.
4. Select *EXIT* to leave the *Report Editor* tool.

Copying a File

You can copy any files displayed in the list box. You must provide a unique name for the file you are copying to.

To copy a file

1. Highlight the file you want to copy in the list box.
2. Select *COPY.*
3. Enter the new filename and extension in the Current File data entry box.
4. Select *EXIT* to leave the *Report Editor* tool.

Printing a File

If you have an online printer, you can print ASCII reports, such as a materials list, by using the *Report Editor.*

To print a file

1. Highlight the file you want to print in the list box.
2. Select *PRINT.*
3. Select *EXIT* to leave the *Report Editor* tool.

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