

Industrial Strength Design Automation Tools in an Introductory Computer Engineering Laboratory

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Abstract

This paper describes our experience with using Mentor Graphics electronic design automation software and Xilinx field programmable gate arrays at the introductory level. The Department of Electrical Engineering at the University of Missouri - Rolla has been a member of Mentor's Higher Education Program for almost ten years. We have been successfully introducing students to the tools by using a series of tutorial exercises in classroom, laboratory, and workshop settings. Until recently however our experience has been mainly with either upper level students including graduate students or with one or two sections of selected classes. Our use of field programmable gate arrays has been limited to upper level design courses. Beginning with the winter 1997 semester we decided to expand our offering and use both industrial strength design automation tools and field programmable gate arrays in all sections of a required introductory computer engineering laboratory.

1. Introduction

The Department of Electrical Engineering at the University of Missouri - Rolla (UMR) has been a participant in the Mentor Graphics Higher Education Program (HEP) since 1989. The HEP has been instrumental in helping us introduce our students to industrial strength electronic design automation tools through our courses [1] [2] and academic research in reconfigurable hardware [3] and smart structures [4]. Our initial involvement with Mentor Graphics (MGC) tools was with their version of SPICE and was used in conjunction with Berkeley's Octtools in an introductory VLSI design course. That success quickly led to the use of MGC's VHDL based logic synthesis tools and Xilinx FPGA's for the project portion of the VLSI design course which previously made use of MOSIS Tinchips and standard cell based designs. The establishment of a Sun workstation based computer

learning center in the EE Department in 1993 made it possible to expand our use of the tools beyond this senior undergraduate and graduate level elective course.

Several short introductory tutorials were developed at UMR to expose students to the industrial strength tools. Needless to say the commercial tools were far from being *user friendly* and could almost be said to be *user hostile*. The usual approach followed with academic tools of turning the students lose with a man page simply would not do. Training courses for the commercial tools typically took an entire 40 hour work week, almost the length of an entire academic semester's length course! We chose to develop simpler tutorials which required little or no instructor intervention, could be worked through in 5 to 10 hours by students working alone or in groups of two, and focused on providing the students with a workable path through the tools without getting involved in all the details or with the intricacies of a complicated circuit. Our tutorials were patterned after the Octtools tutorials developed at the Massachusetts Microelectronics Center.

The availability of easy to follow course materials and a large number of workstations made it possible to consider using the schematic capture and logic simulation tools in our introductory logic design course. This is a required course for all Juniors in EE and Computer Science. Depending upon the whim of each instructor it previously made use of either no EDA tools at all or a variety of ad hoc PC based solutions ranging from free-ware to low cost integrated schematic capture and logic simulation software. Use of the commercial tools on an experimental basis in this required introductory level course was gratifying. The students uniformly appreciated and saw the value in being exposure to *real* tools. Many students were able to build on their experience and use the tools in later courses. The one disappointment is that although new instructors and graduate teaching assistants readily adopt the tools, their enthusiasm isn't shared by more senior faculty.

2. The New Curriculum

Over the past few years the UMR EE Department has been in the process of modifying its curriculum. One such modification has been the abandoning of separate lecture and lab courses with a return to courses with integrated lecture and lab. EE 111 and 112, Introduction to Computer Engineering, is one such. This is a required course for all sophomore EE's. The content of EE 111 is mainly a traditional introductory logic design syllabus while EE 112 is a mixture of schematic capture based logic simulation combined with laboratory verification using real hardware. Based on our own experiences with the use of FPGA's in an introductory course and the experiences of others it was decided to use FPGAs in the new required lab. This was not a decision quickly made. Only one of the lab teaching assistants had any experience with FPGAs. Most of the students had never seen a logic gate before let alone an FPGA. None of the other instructors in the course had any experience with either Mentor software or Xilinx FPGAs. Nevertheless the level of enthusiasm is high and our experience nearly half way through the semester at the time of writing is positive.

The use of design automation tools at this level was not an issue. Our experience over the past several years has led us to the conclusion that no introductory logic design course is really complete without some exposure to logic simulation at the very least. The issue was whether to use FPGA's at this level. The problem is that at least with coarse grain architectures like Xilinx the gate that a student draws on her schematic may or may not have a physical counterpart. What you see is often not what you get. The design issues frequently appear to be at odds with what is being taught in the lecture which often focuses on two level logic minimization with Karnaugh maps. "Why go to all that trouble if the technology mapper rips it all up anyway?" the students ask. The other issue was whether to use schematic capture or HDL based design. We have been using PALASM at this level and the advent of low cost PC based VHDL synthesis tools for PLDs made it tempting to go that route. In the end our desire to stay focused on gate level design and provide a level of motivation through the use of leading edge technology resulted in the decision to use FPGAs for hardware verification of simulation exercises in our required introductory lab.

3. Conclusion

The learning curve for industrial strength design automation tools is not a severe problem. Given a proper process oriented introduction students can come up to speed quickly and begin doing useful work in a matter of

a few hours. The experience gained is not lost effort in that the tools used are not watered down student versions which quickly run out of steam on real designs but are real industrial strength tools capable of handling the largest of systems. They are open ended and can not only be used throughout their academic career, they are likely to be used in industry as well. Students perceive real value in using the same tool that a prospective employer might use and is a motivating factor in learning. By focusing on the design process itself instead of operation of a particular tool students learn concepts of lasting value at the same time they are exposed to industrial quality design aids.

At the time of writing the jury is still out on the use of field programmable gate arrays in an introductory course. Our initial experience is positive but it remains to be seen whether the peculiar design environment offered by FPGAs is appropriate at this level. Is "what you see is not what you get" too distracting to first time designers? Is the motivating force of using leading edge state of the art components the dominant factor? These are two open questions at this point in time.

References

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