

Write Burst Timing Details - 100MHz

Event	Timing (ns) relative to start of CAS cycle				Source
	Worst	Best	Max	Min	
Address becomes valid	-17.0	-17.0	-17.0	-17.0	Measurements
Chip select signal becomes valid	-6.5	-6.5	-6.5	-6.5	Measurements
Data(0) becomes valid	-5.1	-5.1	-5.1	-5.1	Measurements
PAL latch, output enable signals generated	-2.5	-5.5	4.0		1.0 datasheet (Tpd)
CLK goes high	0.0	0.0			Start of cycle 0
PAL latch, output enable reach data buffers	-1.5	-4.5	1.0		1.0 Propagation delay
Data buffers latch incoming data(0)	-0.2	-3.2	1.3		1.3 datasheet (Th)
Next data(1) arrives at buffers	4.6	4.6	4.6		4.6 Measurements
	Data buffer setup time margin	3.6	0.6		
	Data buffer hold time margin	4.8	7.8		
Falling edge of clock	5.0	5.0			2nd half of cycle 0
Next control signals become valid	6.4	6.4	6.4		6.4 Measurements
Data buffer outputs are valid	4.4	1.4	5.9		5.9 Datasheet (Tzh)
Data(0) propagates to SDRAM inputs	5.4	2.4	1.0		1.0 Propagation delay
SDRAM latches incoming data	7.4	4.4	2.0		2.0 Datasheet (Ts)
PAL sends latch disable to data buffers	9.0	6.0	4.0		1.0 Datasheet (Tpd)
PAL latch disable reaches data buffers	10.0	7.0	1.0		1.0 Propagation delay
Data buffer latches disabled	11.2	8.2	1.2		1.2 Datasheet (Tsu)
PAL sends latch enable to data buffers	14.0	8.0	4.0		1.0 Datasheet (Tpd)
Latch enable reaches data buffers			1.0		1.0 Propagation delay
CLK goes high	10.0	10.0			Start of cycle 1